

# SWITCHING REGULATOR DATA BOOK

First in Quality...First in Service • Custom, Semi-custom and Standard IC's



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### Introduction

This Data Book contains a complete summary of technical information covering EXAR's entire line of switching regulator IC products. In addition, several design and application articles are also included, along with a review of fundamentals of pulse-width modulated regulator circuits.

#### **EXPERIENCE AND PRODUCTS**

EXAR's innovativeness, product quality and responsiveness to customer needs have been the key to its success. EXAR today offers a broad line of linear and interface circuits. In the field of standard linear IC products, EXAR has extended its circuit technological leadership into the areas of communications and control circuits. Today, EXAR has one of the most complete lines of IC oscillators, timing circuits and phase-locked loops in the industry. EXAR also manufactures a large family of telecommunication circuits such as tone decoders, compandors, modulators, PCM repeaters and FSK modem circuits. In the field of industrial control circuits, EXAR manufactures a broad line of quad and dual operational amplifiers, voltage regulators, radio-control and servo driver IC's, and power control circuits.

EXAR's experience and expertise in the area of bipolar IC technology extends both into custom and standard IC products. In the area of custom IC's, EXAR has designed, developed, and manufactured, a wide range of full custom monolithic circuits, particularly for applications in the areas of telecommunications, consumer electronics, and industrial controls.

In addition to the full custom capability, EXAR also offers a unique semi-custom IC development capability for low to medium volume custom circuits. This semi-custom program is intended for those customers seeking cost-effective solutions to reduce component count and board size in order to compete more effectively in a changing marketplace. The program allows a customized monolithic IC to be developed with a turnaround time of several weeks at a small fraction of the cost of a full custom development program.

#### **EXCELLENCE IN ENGINEERING**

EXAR quality starts in Engineering where highly qualified people are backed up with the advanced instruments and facilities needed for design and manufacture of custom, semi-custom and standard integrated circuits. EXAR's engineering and facilities are geared to handle all three classes of IC design: (1) semi-custom design programs using EXAR's bipolar, CMOS, and I<sup>2</sup>L Master-Chips; (2) full custom IC design, and (3) development and high-volume production of standard products.

Some of the challenging and complex development programs successfully completed by EXAR include analog compandors and PCM repeaters for telecommunication, electronic fuel-injection, anti-skid braking systems and voltage regulators for automotive electronics, digital voltmeter circuits, 40 MHz frequency synthesizers, high-current and high-voltage display and relay driver IC's, and many others.

#### **NEW TECHNOLOGIES**

Through company sponsored research and development activities, EXAR constantly stays abreast of all technology areas related to changing customer needs and requirements. EXAR has a complete selection of mainstream IC technologies at its disposal. These cover linear and digital bipolar technologies, metal-gate and silicon-gate CMOS and bipolar-compatible integrated injection logic (I<sup>2</sup>L) technologies. EXAR has in-house product and process engineering groups which stay abreast of technological developments in all of these process and fabrication technologies.

#### FIRST IN QUALITY/FIRST IN SERVICE

From incoming inspection of critical materials to the final test of the finished goods, EXAR performs sample testing of each lot to ensure that every product meets EXAR's high quality standards. EXAR's manufacturing process is inspected in accordance with its own stringent Quality Assurance Program, which is in compliance with MIL-I-45208. Additional special screening and testing can be negotiated to meet individual customer requirements.

Throughout the wafer fab and assembly process, the latest scientific instruments are used for inspection and modern automated equipment is used for wafer probe, ac, dc, and functional testing. Burn-in testing of finished products is also done in-house. For special environmental or high reliability burn-in tests, outside testing laboratories are used to complement EXAR's own in-house facilities.

EXAR has the ability and flexibility to serve the customer in a variety of ways, from wafer fabrication to full parametric selection of assembled units for individual customer requirements. Special marking, special packaging and military screening are only a few of the service options available from EXAR. We are certain that EXAR's service is flexible enough to satisfy 99% of your needs. The company has a large staff of Application Engineers to assist the customer in the use of the product and to handle any request, large or small.



## **Fundamentals of Switching Regulators**

In the design of modern electronic equipment and systems, supply voltage regulation is one of the critical circuit functions required for optimum system performance. The function of a voltage regulator is to provide a constant output voltage, under changing line or load conditions

The advent of monolithic IC regulators has greatly simplified power supply design by reducing design complexity, improving reliability and ease of maintenance. Until recently, the field of IC regulators was dominated by linear or "series-pass" type regulators which are easy to use and require a minimum number of external components. However, under changing load and line voltage conditions, series regulators have relatively poor efficiency in power handling: a significant amount of the input power is dissipated, or wasted, in the regulator, particularly under large line input variations.

In many regulator applications, or in power supply designs, the limitations of series regulators can be overcome by using "switching regulator" systems for voltage and power flow control. Although switching regulators require somewhat more complex circuitry external to the chip, they can provide significant improvement in efficiency and versatility over conventional series regulators. Within recent years, power supplies using switching regulators have proliferated greatly, because of improvements in circuit components specifically made for them. Some of these are the inexpensive high-speed switching power transistors, low-loss ferrite cores for inductors and the complex LSI circuits which contain all the critical control circuitry. As a result, the cost and complexity of switching regulator systems have been reduced greatly, making them economically feasible for a wide range of applications.

This data book is intended as a design and applications aid for the circuit designer involved in voltage regulator or power supply design. It covers the basic principles of operation of switching regulator systems, and the monolithic LSI circuits which can be used in designing them.

#### **CLASSES OF IC REGULATORS**

The function of a voltage regulator is to provide a well-specified and constant output voltage level from a poorly specified and sometimes fluctuating input voltage. The output of the voltage regulator would then be used as a supply voltage for the other circuits in the system. In this

manner, the fluctuations and random variations of a supply voltage under changing load conditions are essentially eliminated.

Since the regulation and control of supply voltage is one of the most fundamental and critical requirements of any electronic system design, the monolithic voltage regulator or power control circuits have become one of the essential building blocks of any analog or digital system. As a result, the monolithic voltage regulators, similar to the case of monolithic op amps, have gained wide acceptance and have greatly simplified the tedious task of designing power supply circuits.

Today, there are two very distinctly different types of IC voltage regulators which have gained wide acceptance and popularity. There are the so-called "series regulators" and "switching regulators". The series regulators control the output voltage by controlling the voltage drop across a power transistor which is connected in series with the load. The power transistor is operated in its linear region and conducts current continuously. The switching regulators, on the other hand, control the flow of power to the load by turning on-and-off one or more of the power switches connected in parallel or series with the load, and make use of inductive and capacitive energy storage elements to convert the switched current pulses into a continuous and regulated load current.

#### **SERIES-PASS REGULATORS**

The series or series-pass type voltage regulator is connected in series between the load and unregulated supply line. It is a feedback circuit comprised of three main sections, shown in Figure 1. These are the reference voltage element, the error amplifier and the series-pass element. In most cases, a fourth section, called "overload protection circuitry, is also included in the system to prevent against burn-out under accidental overload conditions.

With reference to the simplified block diagram of Figure 1, the principle of operation of a series regulator can be briefly described as follows: The internal voltage reference generator generates a reference voltage level,  $V_R$ , which is independent of the unregulated supply voltage or the temperature changes. The error amplifier compares  $V_R$  with the sampled and scaled output voltage,  $V_S$ , and generates a corrective error signal to regulate the voltage drop across the pass element such that the  $V_R = V_S$  condition is fulfilled. The scaled voltage,  $V_S$ , is derived from the actual



output voltage by means of the so-called sampling resistors,  $R_1$  and  $R_2$ . If the error amplifier gain is very high, one can show by a simple feedback system analysis that the output voltage is, to a first order, proportional to the reference voltage  $V_B$  and independent of the input voltage:

$$V_{\text{out}} = V_{\text{R}} \left( \frac{R_1 + R_2}{R_2} \right) \tag{2.1}$$

The pass element is normally a high-current transistor, or a Darlington connection of two transistors. Depending on the current and power handling requriements, the pass transistor may be left external to the monolithic IC chip. For proper operation of the pass transistor, it must be biased in its linear region. Therefore, the total voltage drop,  $V_{in}$ - $V_{out}$ , across the pass element must not exceed the breakdown voltage of the pass transistor, and must be greater than a minimum amount, called the drop-out voltage, necessary to keep the pass transistor in its linear or active region.

#### SWITCHING REGULATORS

The switching regulators, which are also called switch-mode regulators, find a wide range of applications in power supply design where high-power and high-efficiency are important. The principle of operation of a switching regulator differs significantly from that of a conventional series regulator circuit. In the case of series regulators, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. In the case of switching regulators, the pass transistor is used in a controlled switch and is operated at either the **cut-off** or the **saturated** state. In this manner, the power is transmitted across the pass device in discrete current pulses, rather than a steady current flow.

The most important advantage of switching regulators over the conventional series regulators is greater efficiency, since the pass device is operated as a low impedance switch. When the pass device is at cut-off, there is no current through it, thus, it dissipates no power. When the pass device is in saturation, it is nearly a short circuit with negligible voltage drop across it; thus, it dissipates only a small amount of average power provided that it can handle the peak current loads. In either case, very little power is wasted in the regulator and pass devices, and almost all the power is transferred to the load. In this manner, a very high degree of regulator efficiency is achieved, typically in the range of 70% to 90%, relatively independent of the input/output voltage differentials. The efficiency of switching regulators is particularly apparent when there is a large input/output voltage difference across the regulator. For example, if one considers the case of a regulator operating with a 28-volt input and delivering a 5-volt output at 1A current, a conventional series regulator would require a drop of 23 volts across the series pass transistor. Thus, a total of 23 watts of power is wasted in the regulator, resulting in an overall regulator efficiency of approximately 18%. As will be described in later sections, a switching regulator can be readily designed to perform the same function with greater than 75% efficiency under similar operating conditions.

Another important advantage of the switching regulator circuits is their versatility; they can provide output voltages which can be less than, greater than, or of opposite polarity to the input voltage, as determined by the mode of operation of the circuit. In this manner, one can stepup, step-down, or invert the polarity of an input voltage to generate any arbitrary set of dc voltages within the power distribution system.

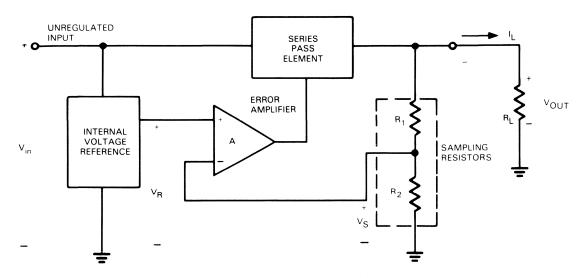


Figure 1. Simplified Block Diagram of a Series Regulator



Switching regulators also have some drawbacks. They are more complex, and require external components such as inductors or transformers. They generate more noise and output ripple than conventional series regulators, and are slower responding to transient load changes. One area of caution, when using switching regulators, is the generation of electromagnetic and radio frequency interference (RFI). This interference problem is usually solved by the use of feedthrough low-pass filters isolating the power lines into the regulator, and by using ground-shields around the regulator to suppress the interference. However, even with these precautions, switching regulator circuits are not recommended for powering very low level signal processing circuitry, where noise characteristics are very critical.

Figure 2 shows the simplified block diagram of a switching regulator power supply system, which comprises several basic blocks. With reference to the figure, the principle of operation of the switching regulator system can be described as follows: The control element is essentially a power switch, which is either "on" (i.e., a virtual short circuit) or "off" (i.e., an open circuit). The duty cycle of the control element is determined by the control logic circuitry, which is driven by an internal oscillator, and puts out periodic control pulses which activate the control pulses (i.e., the on and off duration of the switch over a given period of time is controlled by the output of the error amplifier).

The control element, or switch, delivers pulses of energy into the load circuit which is normally made up of inductive and capacitive components, and diodes. The function of the load circuit is to convert these power pulses to a

steady stream of current flow into an external load resistor,  $R_{\mbox{\scriptsize L}}.$  The voltage level across  $R_{\mbox{\scriptsize L}}$  is sensed by means of a sampling resistor network, and is connected to the input of the error amplifier. The error amplifier compares the sampled output level with that of a reference voltage, and causes the pulse width of the control logic section to vary in such a manner to keep the output voltage level across  $R_{\mbox{\scriptsize I}}$  constant.

The power switch which forms the control element portion of the switching regulator is normally a power transistor which is switched between cutoff and saturation. One advantage of the switching regulator over the conventional linear regulator is greater efficiency, since the cutoff and saturation modes are the two most efficient modes of operation. In the cutoff mode, there is a large voltage across the transistor but little current through it: in the saturation mode, the transistor has little voltage across it but a large amount of current. In either case, little power is wasted, and most of the input power is transferred to the output; therefore, the efficiency is high. Regulation is achieved by varying the duty cycle that controls the average current transferred to the load. As long as this average current is equal to the current required by the load, regulation is maintained.

In addition to high efficiency operation, one added advantage of the switching regulator is the the flexibility of the choice of output voltages available. Depending on the particular load circuit configuration used, the output can be greater than or less than the input voltage, or be of opposite polarity to the input. These features will be explained further in the following sections.

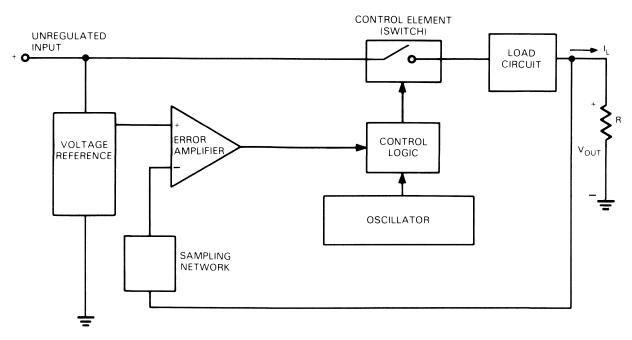


Figure 2. Simplified Block Diagram of a Switching Regulator System



## **Principles of Switching Regulators**

The functional block diagram of a switching regulator circuit is shown in Figure 2. The basic principle of operation of the entire regulator system was qualitatively described in the previous section. Although the switching regulator system contains a large number of subsystems, it can be divided into two major sections:

- a) Control Circuitry
- b) Output Load Circuitry

Control circuitry is comprised of the voltage reference, sampling network, error amplifier, oscillator and the control logic sections shown in Figure 2. The purpose of this circuitry is to control the rate of power flow to the load circuit, and ultimately into the output load, R<sub>L</sub>. The control of power flow is achieved by generating control pulses which determine the on/off period of the control element. The control circuitry normally operates at very low power levels

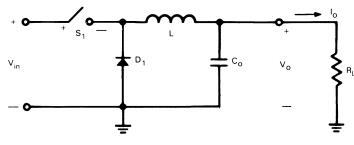
The output load circuitry is made up of the control element and the load circuit. The control element functions as a power switch, and delivers discrete packets of power, in the form of current pulses into the load current. The load circuit converts these into a steady current flow through the external load.

Depending on the type of output load circuitry used, switching regulator power supplies can be classified into three categories. These are:

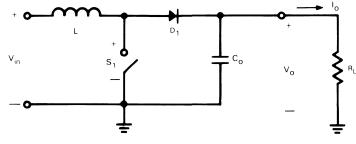
- 1. Single-ended inductor circuits.
- 2. Diode/Capacitor circuits.
- 3. Transformer coupled circuits.

Figure 3 shows the three basic configurations for the output circuitry of single-ended inductor type switching regulators. These are among the most frequently used output circuit configurations since they are by far the easiest to design and control for medium and high-current applications.

Figure 4 shows the switching regulator configurations using diode/capacitor circuits. These circuits are typically used for very low current applications, and primarily as voltage multipliers, to increase the voltage level available from a low voltage battery. Examples of such applications are the generation of voltage drive for LCD displays in watch circuits from a 1.5-volt or 3-volt battery, and in low voltage hearing aid amplifiers.



(a) STEP-DOWN CONFIGURATION (V  $_{\rm in}$  > V  $_{\rm o}$ )



(b) STEP-UP CONFIGURATION ( $V_0 > V_{in}$ )

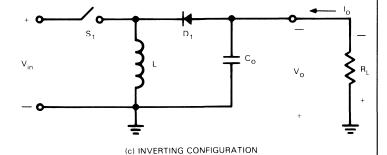


Figure 3. Single-Ended Inductive Load Circuits



Figure 5 shows the two basic configurations of transformer coupled output circuits. The circuit of Figure 5(a) is the so-called push-pull circuit used in conventional dcto-dc converters, with each switch controlled for 0 to 45% duty cycle modulation. The configuration of Figure 5(b) is the so-called single-ended flyback converter, which is useful at low-to-medium current loads.

The design of power supply systems using discrete circuits and the various types of output circuitry shown in Figures 3 through 5 are well covered in the literature. In the following discussions, we will primarily focus on switching regulator circuits using the single-ended inductor type output circuit shown in Figure 3, since these represent by far the most common category of application.

The control circuitry section of a switching regulator system, which controls the on/off duty cycle of the switch transistors, can be readily integrated in a monolithic IC form. In many cases, the switching transistors up to 1A current rating can also be incorporated into the monolithic chip. If higher power levels are required, the switch transistor on the chip is used as a drive for an external high current switch.

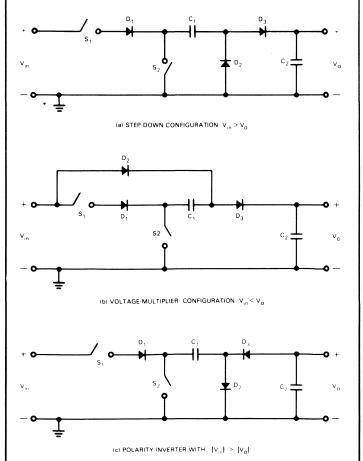
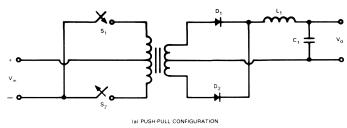


Figure 4. Diode/Capacitor Type Load Circuits

Figure 6 shows a simplified block diagram of a typical switching regulator IC used in conjunction with the single-ended inductor configuration of Figure 3(a). The circuit generates a stream of pulses which turn switch  $S_1$  "on" and "off". The output dc level is sensed through the sampling resistors,  $R_1$  and  $R_2$ , and compared against an internal voltage reference,  $V_{ref}$ , with the on/off time on the duty cycle of the switch,  $S_1$ , varied accordingly to keep the output voltage constant under changing load conditions.

Neglecting the current in the sampling resistors, the average or dc value of the output current,  $I_0$ , delivered to the load is proportional to the duty cycle of the power switch,  $S_1$ , as illustrated in Figure 7. If the sampled output voltage is lower than  $V_{ref}$ , the polarity of the comparator output signal causes the control logic to increase the duty cycle of  $S_1$  and, thus, causes the output voltage level to increase until the equilibrium is reached such that the output voltage, scaled down by the sampling resistors, is equal to the internal reference voltage. Similarly, if the output load current,  $I_0$ , is decreased, this would cause the output voltage to increase which in turn would be sensed by the control circuitry and would reduce the duty cycle of the switch accordingly.



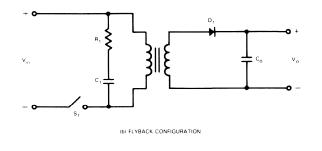


Figure 5. Transformer Coupled Load Circuits



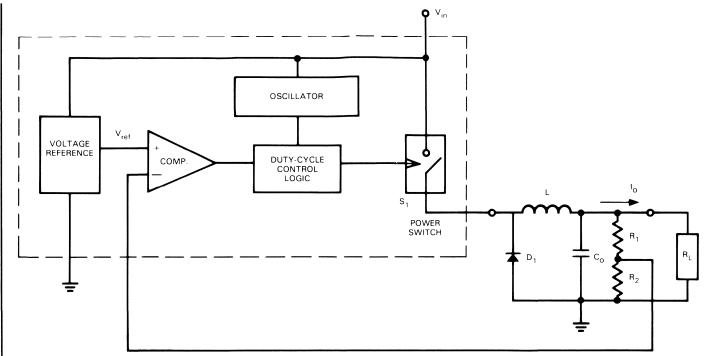


Figure 6. Simplified Block Diagram of a Switching Regulator IC in "Step-Down" Configuration

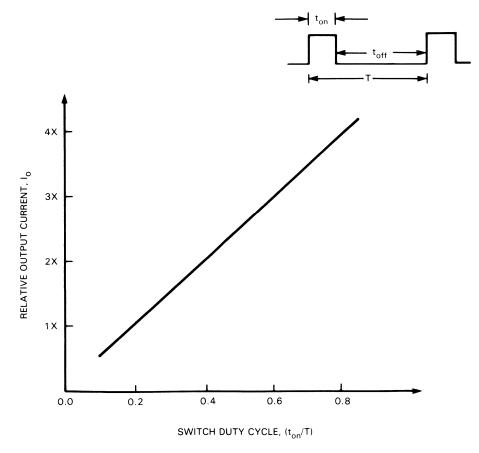


Figure 7. Output Load Current,  $I_0$ , as a Function of Switch Duty Cycle



## **Methods of Duty Cycle Control**

The switch duty cycle,  $(t_{On}/T)$ , can be controlled by pulse width modulation at a fixed frequency, or by fixing the "on" or "off" time, and varying the frequency. The relative merits and disadvantages of these techniques are briefly examined below.

#### (a) Fixed Frequency, Variable Duty Cycle Operation:

In this type of a switching regulator, the operating frequency is fixed and the duty cycle of the pulse train is varied to change the average power. This method is often referred to as pulse width modulation (PWM). The fixed frequency concept is particularly advantageous for systems employing transformer coupled output stages. The fixed frequency aspect enables the efficient design of the associated magnetics. In addition, filtering or shielding the surroundings from the radio frequency or electromagnetic interference generated by the regulator is somewhat simplified because of the fixed frequency of switching. Because of these features, the majority of the switching regulator control IC's utilize a fixed frequency, variable duty cycle control method.

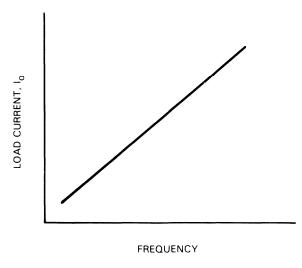
#### (b) Fixed On-Time, Variable Frequency:

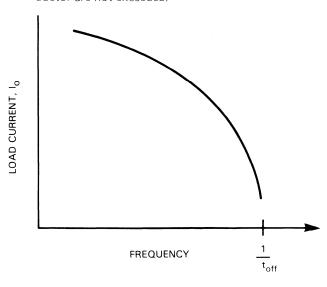
In this method, the switch has a fixed or predetermined "on" time, and the duty cycle is varied by varying the frequency or repetition rate of the control pulses. This methods provides ease of design in voltage conversion applications using the single-ended

inductive output circuit configurations of Figure 3, and simplifies design calculations for the inductor value. The fixed on-time method is also advantageous for inductive output circuitry, since a consistent amount of charge is developed in the inductor during the fixed on-time. This eases the design or the selection of the inductor by defining the operating area to which the inductor is subjected under transient load conditions. Figure 8(a) shows the typical frequency vs. load current characteristics of a fixed on-time, variable frequency regulator, where the frequency increases linearly with increasing load.

#### (c) Fixed Off-Time, Variable Frequency:

In this type of a voltage regulator, the dc voltage at the output is varied by changing the on-time, ton, of the switch, while maintaining a fixed off-time, toff. As shown in Figure 8(b), the fixed off-time switching regulator behaves in an opposite manner to the fixed on-time system; as the load current increases, the ontime becomes longer, thus decreasing the frequency. This approach is advantageous for the design of a switching regulator which will operate at a welldefined minimum frequency and low ripple current under full load conditions. One basic drawback of the fixed off-time system is that the maximum current in the inductor, under transient load conditions, is not well-defined. Thus, additional care is required to ensure that the saturation characteristics of the inductor are not exceeded.





(a) FIXED ON-TIME

(b) FIXED OFF-TIME

Figure 8. Typical Load Current vs Frequency Characteristics of (a) Fixed On-Time and (b) Fixed Off-Time Variable Frequency Switching Regulators



## Modes of Operation with Inductive Output Circuits

Two of the most important advantages of switched regulators are their high efficiency and their ability to step-up step-down, or change polarity of an input voltage. These basic features can be best understood by examining the voltage and current waveforms at the output of the regulator. In this section, some of the waveforms and key design equations associated with the inductive output circuits of Figure 3 will be examined for various modes of operation under steady-state load conditions. For the sake of brevity, rigorous derivations will be omitted and only their conclusions will be presented.

#### STEP-DOWN OPERATION

In the step-down operation, the switching regulator produces an output dc voltage,  $V_0$ , which is lower than the input voltage,  $V_{1n}$ . Figure 9 shows the basic voltage and current waveforms associated with the circuit under steady-state operation. The switch,  $S_1$ , is assumed to have a voltage drop of  $V_{Sat}$  in its "on" condition, and the diode,  $D_1$ , has a forward drop of  $V_D$  when it is conducting.

When  $S_1$  is closed, or on,  $D_1$  is off, and the current in the inductor,  $I_{PK}$ , rises linearly from zero to its peak value,  $I_L$ , with the slope:

$$\frac{dI_L}{dt} = \frac{V_L}{I} = \frac{V_{in} - V_{sat} - V_O}{I}$$
 (4.1)

At the end of the switch on-time,  $t_{On}$ , this current reaches its maximum value, IpK. When S1 is off, the inductor generates the necessary voltage to forward bias D1, and keep IL from changing instantaneously. During this portion of the cycle, IL linearly decays to zero at the end of the off-time  $t_{Off}$ .

At steady-state, average or dc current through  $C_0$  is zero, therefore, the output dc current,  $I_0$ , is equal to the average value of  $I_1$ , or:

$$I_0 = (I_L)_{aug} = \frac{I_{pk}}{2}$$
 (4.2)

From the waveforms shown in Figure 9, the switch "on" and "off" times can be related to the voltage levels at the input and output of the circuit, as:

$$\frac{t_{On}}{T_{Off}} = \frac{V_O + V_D}{V_{in} - V_{sat} - V_O}$$
 (4.3)

or, Vo, can be to the rest of the voltages as:

$$V_O = (\frac{t_{OI}}{T}) (V_{in} - V_{sat}) - (\frac{t_{Off}}{T}) V_D$$
 (4.4)

assuming an ideal case where both the saturation and diode voltages are zero or negligible, this reduces to:

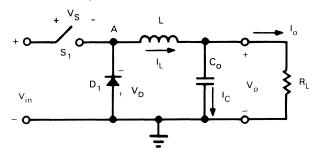
$$(V_0)_{ideal} = (\frac{t_{on}}{T}) V_{in}$$
 (4.5)

Equation (4.5) implies that, ideally, the switching regulator in its step-down mode provides a down scaling of the input voltage by a scale factor equal to the duty cycle of the switch transistor.

Another important parameter of the step-down regulator is the peak-to-peak output ripple voltage,  $(\Delta V_0)_{pp}$ . Assuming that  $C_0$  is sufficiently large so that the ripple voltage is much lower than the average or dc value of the output,  $(\Delta V_0)_{pp}$  can be expressed as:

$$(\Delta V_0)_{pp} = \frac{lpk}{8C_0} (t_{on} + t_{off}) = \frac{lpk}{8C_0}$$
 (4.6)

where f = 1/T is the frequency or the repetition rate at which the switch opens and closes.



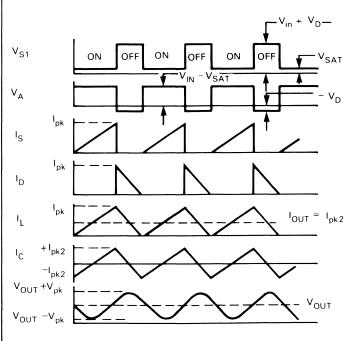


Figure 9. Switching Regulator Voltage and Current
Waveforms in Step-Down Mode



#### STEP-UP OPERATION

In the step-up mode the switching regulator produces an output dc voltage  $V_0$ , which is higher than  $V_{in}$ . The circuit configuration for this mode of operation, along with the associated voltage and current waveforms, is shown in Figure 10 under steady-state operation.

With reference to Figure 10, the operation of the circuit can be summarized as follows: Assuming that S<sub>1</sub> is open and closes at the moment IL = 0, the current in the inductor rises linearly from zero to a peak value, IPK, during ton. At the end of on-time, S1 is opened. Since II cannot change instantaneously, the inductor generates the necessary voltage at node A to forward-bias D1, and keep the current continuous. During the off-time, II decays linearly, and reachs zero at toff. Then, S1 closes again, and the cycle repeats itself. While D1 is conducting, it supplies current to both the hold and the loading capacitor, Co; when D<sub>1</sub> is nonconducting, the output current is drawn from Co. Note that at steady-state, the average or dc current through D<sub>1</sub> is equal to the output or load current, IL, and the net charge supplied to CO, per cycle of operation, is zero.

The peak current, IPK, is related to the steady-state output current as:

$$I_{pk} = 2 I_0 \left( \frac{V_D + V_0 - V_{sat}}{V_{in} - V_{sat}} \right)$$
 (4.7)

and the on/off times of the switch, necessary for IL to ramp from zero to IpK and back to zero, are related as:

$$\frac{t_{On}}{T_{Off}} = \frac{V_D + V_O - V_{sat}}{V_{in} - V_{sat}}$$
 (4.8)

Solving Eq. (4.8) for  $V_O$ , one obtains:

$$V_0 = V_{in} \left(\frac{T}{t_{off}}\right) - V_{sat} \left(\frac{t_{on}}{t_{off}}\right) - V_D$$
 (4.9)

where  $T(=t_{On} + T_{Off})$  is the period of one full cycle of operation. In the idealized case, where the diode drop and  $V_{sat}$  of the switch are negligible, Eq. (4.9) reduces to:

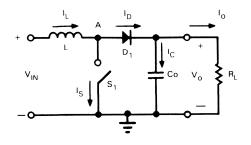
$$(V_0)_{ideal} = V_{in} \left(\frac{T}{t_{off}}\right)$$
 (4.10)

or, in other words, the step-up mode of operation results in up-scaling the input voltage by the ratio  $(T/t_{Off})$ .

The peak-to-peak output ripple voltage can be expressed as:

$$(\Delta V_0)_{pp} = \frac{(I_{pk} - I_0)^2}{2 I_{pk}} (t_{off} / C_0)$$
 (4.11)

with the assumption that  $(\Delta V_0) \ll V_0$ .



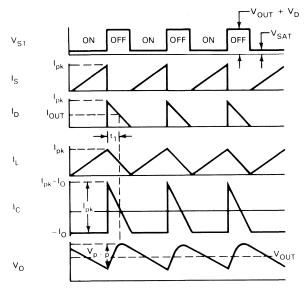


Figure 10. Voltage and Current Waveforms in Step-Up
Mode

#### POLARITY-INVERTING OPERATION

In the polarity-inverting mode of operation, the switching regulator produces an output voltage across the load which is the opposite polarity to the input. Figure 11 shows the basic circuit configuration for this mode of operation. The polarity inversion is achieved by making the inductor force a current in the opposite direction through the load.

The operation of the circuit can be briefly described as follows: The current, IL, through the inductor ramps up from zero to IpK during  $t_{OR}$ , and ramps down to zero during  $t_{Off}$ , similar to the other two modes of operation described earlier. During  $t_{Off}$ , with S1 open, the inductor generates a negative voltage at node A to forward bias D1 and keep IL continuous. As in the case of step-up circuits, the average value of the diode current, ID, is the steady state load current IO, since CO cannot pass any dc current Thus, from the waveforms and timing relations of Figure 11, one can express the peak current, IpK, as:

$$I_{pk} = 2 I_0 \left( \frac{V_{in} + V_D - V_o - V_{sat}}{V_{in} - V_{sat}} \right)$$
 (4.12)



and the on/off times of the switch, necessary for IL to ramp up from zero to  $\mbox{\rm IP}_{\mbox{\it K}}$  and back to zero, arc:

$$\frac{t_{OI}}{t_{Off}} = \left(\frac{V_D - V_O}{V_{in} - V_{sat}}\right) \tag{4.13}$$

Solving the above equation for  $V_0$ , one gets:

$$V_0 = -[(t_{on}/t_{off})(V_{in} - V_{sat}) - V_D]$$
 (4.14)

In the idealized case, where  $V_{\mbox{\scriptsize D}}$  and  $V_{\mbox{\scriptsize Sat}}$  are neglected, Eq. (4.14) will reduce to:

$$(V_0)_{ideal} = -(\frac{t_{0n}}{t_{0ff}}) V_{in}$$
 (4.15)

or in other words, the polarity-inverting mode of operation results in the reversal of polarity of the output voltage as well as its being scaled by the  $(t_{On}/t_{Off})$  ratio.

The peak-to-peak output ripple,  $(\Delta V_0)_{pp}$ , associated with the inverting operation can be expressed as:

$$(\Delta V_{O})_{pp} = \frac{(I_{pk} - I_{O})^{2}}{2 I_{pk}} (\frac{t_{off}}{C_{O}})$$
 (14.16)

which is identical to the case of step-up operation (see Eq. 4.16).

One word of caution is in order when using the polarity inverting configuration: Since the output polarity is reversed, the feedback polarity from the sampling resistors to the voltage comparator in the control circuitry (see Figure 6) must be reversed. Normally, this is done by reversing the reference and feedback inputs into the voltage comparator.

#### **EFFICIENCY CONSIDERATIONS**

The efficiency of a voltage regulator is defined as the ratio of the output power to the input power, i.e.:

Regulator Efficiency = 
$$\eta = \frac{P_O}{P_{in}}$$
 (5.1)

where  $P_0$  is the power delivered to the load, and  $P_{1n}$  is the power drawn from the power lines.

The efficiency advantage of switching regulator circuits can be illustrated best by comparing their efficiency with that of a series-pass type regulator.

#### Efficiency of a Series Regulator

In calculating the efficiency of a series regulator, similar to that shown in Figure 1, one can use a simple equivalent model of power dissipation within the regulator, as shown in Figure 12.

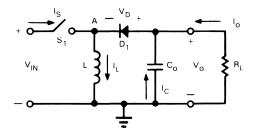
In this model, the current source, IB, represents the total bias and operating current consumed in the regulator circuitry, and VB represents the voltage drop across the pass transistor. For proper operation of the circuit, VB is restricted to be greater than the drop-out voltage.

From the simple model of Figure 12, the input and output power levels can be written as:

$$P_{in} = V_{in} (I_B + I_L)$$
 (5.2)

and

$$P_{O} = V_{O} I_{I} \tag{5.3}$$



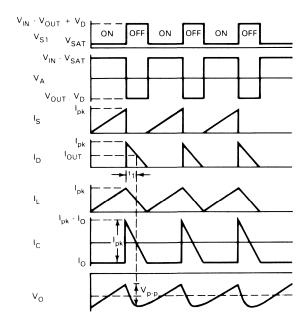


Figure 11. Voltage and Current Waveforms in Polarity-Inverting Mode



Then, the efficiency,  $\eta$ , can be expressed as:

$$\eta = \frac{P_{O}}{P_{In}} = \frac{1}{(1 + V_{B}/V_{O})(1 + I_{B}/I_{L})}$$
(5.4)

As given by Eq. (5.3), regulator efficiency depends directly on the ratio of load voltage and load current to the bias voltage and bias current. Since the bias current, IB, is more or less fixed by the regulator design, the maximum rated efficiency,  $\eta$ , is obtained when the regulator is delivering its maximum rated current with the minimum input/output voltage differential. If the input contains large ac components, or large minimum/maximum flucuations, the maximum efficiency is reduced since the average level of the input voltage would have to be increased to ensure that the instantaneous value of VB is greater than the drop-out voltage.

#### **Efficiency of Switching Regulators**

Starting with the basic definition of efficiency given in Eq. (5.1), one can obtain the expressions for switching regulator efficiency under various operating modes.

For the case of the step-down regulator circuit, one can derive, from Eq. (4.2) through (4.4), an experession for efficiency as:

$$(\eta)_{\text{step-down}} = (\frac{V_0}{V_0 + V_D}) \left( \frac{V_{\text{in}} + V_D - V_{\text{sat}}}{V_{\text{in}}} \right)$$
 (5.5)

In a similar manner, the efficiency expression for step-up operation can be derived from Eq. (4.7) through (4.9) as:

$$(\eta)_{\text{step up}} = (\frac{V_0}{V_0 + V_D - V_{\text{sat}}}) (\frac{V_{\text{in}} - V_{\text{sat}}}{V_{\text{in}}})$$
 (5.6)

The efficiency expression for inverted polarity operation can be derived from Eq. (4.12) through (4.14) as:

$$(\eta)_{\text{inverter}} = (\frac{|V_{\text{OI}}|}{|V_{\text{D}}| + |V_{\text{OI}}|}) (\frac{|V_{\text{in}} - V_{\text{sat}}|}{|V_{\text{in}}|})$$
(5.7)

The efficiency expressions given above do not take into account the quiescent power dissipation in the control circuitry, which can cause the efficiency to decrease at very low current levels, when the average input current is of the same order of magnitude as the quiescent current. The switching transient losses in the switch transistor and diode, as well as the parasitic resistances associated with the inductor, are also not included in the above expressions. In practical regulator systems, these latter losses will cause small but finite reduction in the observed efficiency as compared to the theoretical results given in Eq. (5.5) through 5.7). The exact nature of this reduction in efficiency depends on the specific transistor, diode and inductor characteristics used, as well as on the selection of operating frequency.

There are two additional observations which can be made regarding the efficiency expressions:

- 1. In the ideal case, where both  $V_{\text{Sat}}$  and  $V_{\text{D}}$  go to zero, all three regulator configurations provide an ideal efficiency of 100%.
- 2. The efficiency expressions of Eq. (5.5) through (5.7) are not sensitive to input/output voltage differential across the regulator. This is very different than the case of a conventional series regulator where efficiency varies inversely with the input/output voltage differential (see Eq. 5.4).

As an illustration, it is worthwhile comparing the efficiency of a power supply system with a 20-volt input and a 5-volt output with a conventional series regulator, to that with a step-down switching regulator. For simplicity, quiescent power dissipation associated with the control circuitry will be neglected.

In the case of a conventional series regulator, the efficiency is:

$$(\eta)_{\text{series}} \approx \frac{5}{20} = 25\%$$
 (5.8)

For the case of a step-down regulator, assuming typical values of  $V_D$  = 1 volt, and  $V_{sat}$  = 1.5 volts, one gets from Eq. (5.5):

$$(\eta)_{\text{switching}} = (5/6) \left( \frac{19.5}{20} \right) = 81.25\%$$
 (5.9)

which illustrates one of the most important features of switching regulators namely efficient transfer of power.

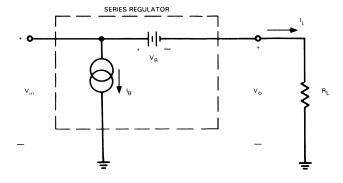


Figure 12. A Simplified Model for Calculating Efficiency of a Series Regulator



## Stability Considerations in Switching Regulato

Similar to the case of conventional regulators, switched-mode power supplies are operated as closed-loop feedback systems; the output voltage level is constantly sensed, and a corrective signal is generated via a negative feedback path to keep it very nearly constant under varying load conditions. Since the overall regulator is a feedback system, it must be designed to meet certain stability criteria in order to assure its proper operation.

As in all feedback systems, the switching regulator circuits must also meet the so-called "Nyquist Criteria" for stability; namely the total phase shift around the regulator feedback loop must be less than -180 degrees when the total loop gain is unity (i.e., 0 dB). Stated in another way, this criteria also states that the loop gain must be less than zero dB when the phase shift reaches -180 degrees.

A convenient parameter to measure the margin of stability in a switching regulator is the so-called phase margin, which is defined as the amount of margin left in degrees before the phase reaches -180 degrees, at the frequency-where the gain is equal to zero dB. For example, if the total phase shift around the feedback-loop is -130 degrees when the gain reaches unity, this corresponds to a phase margin of 50 degrees.

The higher the phase margin, the higher is the margin of stability. However, if the phase margin is too high, the system response tends to be too slow and sluggish. As a general rule, a phase margin of approximately 45 degrees is desireable for maximum stability.

In order to investigate the stability in a switching regulator, it is usually necessary to examine the gain and phase shift characteristics of each of the functional blocks that

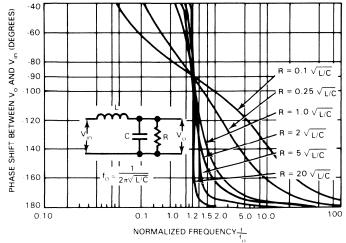


Figure 13. Phase Shift vs Frequency for Switching
Regulator LC Filter

make up the system. Then a gain and phase vs. frequency plot is constructed for each block and combined to generate a composite frequency response of the total system. The gain of each block can be added algebraically (in dB) to obtain the overall loop gain. Then, the combined gain and phase characteristics can be examined to calculate the overall phase margin. If the overall phase margin is less than 45 degrees, it is usually necessary to modify the system to enhance its stability.

The functional blocks which contribute most of the loop gain and phase shift are the error amplifier and the output LC filter. However, the sampling network and pulse width modulator must also be considered.

Gain and phase shift of the LC network is of most importance since it contributes most of the phase shift in the loop. Figure 13 shows a plot of phase shift vs. frequency for an LC filter. Note that with high values of  $(R/\sqrt{LC})$ , the phase shift approaches –180 degrees. Figure 14 shows a plot of gain vs. frequency for the same filter. For high values of  $(R/\sqrt{LC})$ , the resonant peak becomes dominant.

Gain and phase plot of the error amplifier are usually provided in the manufacturer's data sheet. By tailoring the feedback network around the amplifier, it is possible to alter the closed loop frequency response for improved stability. There are various compensation and feedback techniques, such as lead, lag, and integrating networks, that will produce different gain and phase responses.

The sampling network in most switched mode power supplies is usually a resistive network to level shift the output voltage to a suitable range for the error amplifier. This contributes some voltage attenuation but no phase shift.

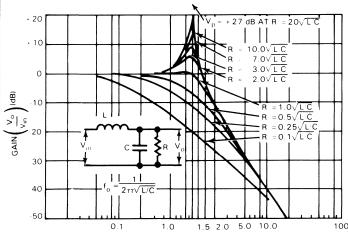


Figure 14. Gain vs Frequency for Switching

Regulator LC Filter



## **Selection of External Components**

Switching regulator systems require the use of external inductors, capacitors, switching transistors, and diodes, in addition to the basic controller IC chip. In this section, some of the requirements of design and selection criteria for these external components shall be reviewed.

#### Selecting the Inductors

In the selection of the inductor, one important criteria is the choice of the core material. The core must provide the desired inductance without saturating magnetically at the maximum peak current. In this respect, each core has a specific energy storage capability,  $\rm LI^2_{Sat}$ , where  $\rm I_{Sat}$  is the magnetic saturation current of the inductor.

The window area for the core winding must permit the number of turns necessary to obtain the required inductance with a wire size that has acceptable dc losses in the winding at maximum peak current. Each core has a specific dissipation capability, LI<sup>2</sup>, that will result in a specific power loss or temperature rise. This temperature rise, plus the ambient temperature, must not exceed the Curie temperature of the core.

The value of the inductance, L, can be related to the basic core parameters and the total number of turns, N, in the wound core as:

$$L = N^2 \times 0.4 \,\pi \,\mu \,A_e \,I_e \times 10^{-5} \tag{7.1}$$

where:

 $\mu$  = effective permeability of core ee = effective magnetic path length (cm) Ae = effective magnetic cross section (cm<sup>2</sup>)

Another useful inductor parameter is the inductor index,  $A_L$ , which is defined as:

$$A_1 = 0.4 \pi \mu A_e I_e \times 10 \text{ (mH/1000 turns)}$$
 (7.2)

From these equations, the magnetic energy,  $(LI^2)$ , stored in the core at a given current level can be written as:

$$L_12 = (N_1)^2 (A_1 \times 10^{-6}) \text{ (millijoules)}$$
 (7.3)

The maximum ampere turn capability, (NI), of a given inductor is limited by the magnetic saturation of the core material. If the inductor index,  $A_L$ , and the saturation current,  $I_{sat}$ , are given for a particular inductance value, the maximum ampere turns can be calculated from Eq. (7.3).

If the saturation flux density,  $B_{\text{sat}}$ , is given, then the maximum energy which can be stored in the inductor can be expressed as:

$$LI2 = \frac{(BSAT)^2 (A_e^2 \times 10^{-4})}{A_L}$$
 (millijoules) (7.4)

The core selected for an application must have an LI2<sub>sat</sub> value greater than calculated, to insure that the core does not saturate under maximum peak current conditions.

In switching regulator applications, power dissipation in the inductor is almost entirely due to dc losses in the winding. The dc resistance of the winding,  $R_{\rm W}$ , can be calculated as:

$$R_{W} = P(I_{W}/A_{W})) N \qquad (7.5)$$

where:

P = resistivity of wire  $(\Omega/cm)$ 

w = length of turn (cm)

 $A_{w}$  = effective area of wire (cm<sup>2</sup>)

Core geometry provides a certain window area,  $A_C$ , for the winding. The effective area,  $A_C'$ , is 0.5  $A_C$  for toroids and 0.65  $A_C$  for pot cores. Equation (7.6) relates the number of turns, area of wire, and effective window area of a fully wound core:

$$A_W = A'_C/N \text{ (cm2)}$$
 (7.6)

From Eq. (7.5) and (7.6), the power dissipation,  $P_{W}$ , in the inductor winding can be calculated as:

$$P_W = I^2 R_W = I^2 P \frac{I_W}{A'_C} N^2$$
 (7.7)

Substituting for N and rearranging:

$$L_1 = P_W \frac{A_L A_C}{P_{W}} \times 10^{-6} \text{ (millijoules)}$$
 (7.8)

Equation (7.8) shows that the LI<sup>2</sup> capability is directly related to and limited by the maximum permissible power dissipation. One procedure for designing the inductor is as follows:

- Calculate the inductance, L, and the peak current, IPK, for the application. The required energy storage capability of the inductor, LI2<sub>PK</sub>, can now be defined (7.4) or (7.8),
- 2. Next, from Eq. (0.0) or (0.0), calculate the maximum  $\mbox{LI}^2_{\mbox{sat}}$  capability of the selected core, where:

$$LI^2_{sat} > LI^2_{PK}$$



- 3. From Eq. (7.1), calculate the number of turns, N, required for the specified inductance, L, and finally, from Eq. (7.5), the power dissipation,  $P_W$ .  $P_W$  should be less than the maximum permissible power dissipation of the core.
- 4. If the power losses are unacceptable, a larger core or one with a higher permeability is required, and steps 1 through 3 will have to be repeated.

Several design cycles are usually required to optimize the inductor design. With a little experience, educated guesses as to core material and size come close to requirements.

#### **Selection of Switching Components**

The designer should be fully aware of the capabilities and limitations of power transistors used in switching applications. Transistors in linear applications operate around a quiescent point, whereas in switching applications, operation is fully on or fully off. Transistors must be selected and tested to withstand the unique stress caused by this mode of operation. Parameters such as current and voltage ratings secondary breakdown ratings, power dissipation, saturation voltage and switching times, critically affect transistor performance in switching applications. Similar parameters are important in diode selection, including voltage, current, and power limitations, as well as forward voltage drop and switching speed.

Initial selection can begin with the voltage and current requirements. Voltage ratings of the switching transistor and diode must be greater than the maximum input voltage including any transient voltages that may appear at the input of the switching regulator. Transistor saturation voltage, VCE<sub>(sat)</sub>, and diode forward voltage, VD, at full load output current should be as low as possible to maintain high operating efficiency. The transistor and diode should be selected to handle the required maximum peak current and power dissipation.

Good efficiency requires fast switching diodes and transistors. Transistor switching losses become significant when the combined rise,  $t_r$ , plus fall time,  $t_f$ , exceeds:

$$0.05 (t_{on} + t_{off})$$

For 20 kHz operation,  $t_r$  +  $t_f$  should be less than 2.5  $\mu$ s for maximum efficiency. While transistor delay and storage times do not affect efficiency, delays in turn-on and turn-off can result in increased output voltage ripple. For optimal operation, combined delay time,  $t_d$ , plus storage time,  $t_s$ , should be less than:

$$0.05 (t_{on} + t_{off})$$

#### Selection of Filter Capacitors

In general, output capacitors used in switching regulators are large (> 100  $\mu$ F), must operate at high-frequencies (> 20 kHz), and require low ESR and ESL. An excellent trade-off between cost and performance is the solid tantalum capacitor, constructed of sintered tantalum power particles packed around a tantalum anode, which makes a rigid assembly or slug. Compared to aluminum electrolytic capacitors, solid tantalum capacitors have higher CV product-per-unit volume, are more stable, and have hermetic seals to eliminate the effects of humidity.

#### Reducing Electromagnetic Interference (EMI)

Due to the wiring inductance in a circuit, rapid changes in current generate voltage transients. These voltage spikes are proportional to both the wiring inductance and the rate at which the current changes:

$$V = -L \frac{di}{dt}$$

The energy of the voltage spike is proportional to the wiring inductance and the square of the current:

$$E = 1/2 LI^2$$

Interference and voltage spiking are easier to filter, if the energy in the spikes is low and the components predominantly high-frequency.

To minimize the EMI problem, the following precautions are recommended:

- Keep loop inductance to a minimum by utilizing appropriate layout and interconnect geometry.
- Keep loop area and lead lengths as small as possible and, in step-down mode, return the input capacitor directly to the diode to reduce EMI and ground-loop noise.
- Select an external diode that can hold peak recovery current as low as possible. This reduces the energy content of the voltage spikes.



## Features & Capabilities

FEATURES / CAPABILITIES	XR-494	XR-495	XR-1524 XR-2524 XR-3524	XR-1525A XR-2525A XR-3525A	XR-1527A XR-2527A XR-3527A	XR-1543 XR-2543 XR-3543	XR-2230	XR-4194	XR-4195
Pulse Width Modulating	×	×	×	×	×		×		
Maximum Frequency (Guaranteed)				400kHz	400 kHz		100kHz		
Maximum Frequency (Typical)	300 kHz	300kHz	300kHz						
Linear Ramp Oscillator	×	×	×	×	×		×		
Capacitor Charge Oscillator									
Deadtime Adjustment (Freq. Dependent)			×	×	×				-
Independent Deadtime Adjustment	×	×					×		
Maximum Input Voltage	407	400	407	35V	35V	407	±15V	+45	∓30
Minimum Input Voltage	77	7	8V (4.5V)	88	8	4.5V	±10V	Vo+2V	Vo+2V
Output Current Capability	200mA	200mA	100mA	200mA	200mA		30mA	150mA	100mA
Single Ended Output								×	×
Double Ended Output	×	×	×	×	×		×	×	×
Totem Pole Output				×	×				
Internal Soft Start				×	×				
External Soft Start Capability	×	×	×				×		
Internal Current Sense Amplifier	×	×	×			×	×		
Internal Reference Voltage	5.0V	5.0V	5.00	5.17	5.17	2.5V		×	×
Internal Precision Reference				×	×	×			
Error Amp	×	×	×	×	×		×	×	×
Under-Voltage Sense/Lockout				×	×	×			
Over-Voltage Sense						×			
External Shutdown Control			×	×	×	×			
SCR Trigger Capability						×			
Double Pulse Protection	×	×		×	×		×		

## **EXAR Switching Regulator Products**



## Pulse-Width Modulating Regulator

#### **GENERAL DESCRIPTION**

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip in the XR-494. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transitors. Single-ended or push-pull output operation may be selected through the output control function. The XR-494 architecture prohibits the possibility of either output being pulsed twice during push-pull operation. The internal amplifier's circuitry allows for a common-mode input voltage range of -0.3 volts to V<sub>CC</sub> -2 volts. The deadtime control comparator provides approximately 5% deadtime unless the dead-time control is externally driven.

#### **FEATURES**

Complete PWM Power Control Circuitry
Uncommitted Outputs
for 200-mA Sink or Source
Output Control Selects Single-Ended
or Push-Pull Operation
Internal Circuitry Prohibits Double Pulse
at Either Output
Variable Dead-time
Circuit Architecture
Provides Easy Synchronization
Current Limiting Capability

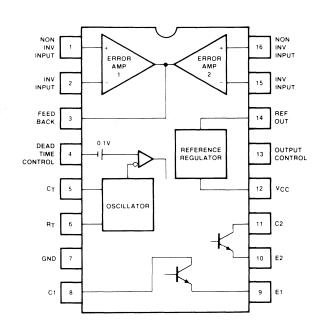
#### **APPLICATIONS**

Power Control Systems Switching Regulators

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, VCC	41 V
Collector Output Voltage	41 V
Amplifier Input Voltage	VCC +0.3V
Collector Output Current	250 mA/each
Power Dissipation 25°C	
Ceramic Package	1000 mW
Derate Above +25°C	8 mW/°C
Plastic Package	625 mW
Derate Above +25°C	5.0 mW/°C
Operating Junction Temperature, T <sub>J</sub>	150°C
Storage Temperature	-65°C to +150°C

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Part Number	Package	Operating Temperature
XR-494M	Ceramic	-55°C to +125°C
XR-494CN	Ceramic	$0^{\circ}$ C to $+70^{\circ}$ C
XR-494CP	Plastic	0°C to +70°C

#### SYSTEM DESCRIPTION

The XR-494 Pulse-width Modulator contains all the necessary control functions for a high-performance switching regulator. The XR-494 can be used in step-down, step-up, and inverting configuration, as well as transformer-coupled flyback and push-pull modes with a minimum number of components. Current limiting is possible by using either error amplifier provided on the XR-494. Soft-start function can be achieved by connecting an RC network between the V<sub>ref</sub> and the dead-time control pins. The dead-time pin can also be used for over-voltage protection by using a shunt regulator. The output control input must be grounded for single-ended output operation (both inputs tied in parallel). For push-pull configuration, this pin must be tied to the internal 5V reference. Multiple units can be easily synchronized to an external source by providing a sawtooth waveform to the CT terminals, and by terminating the RT pin to the reference output.



#### **ELECTRICAL CHARACTERISTICS**

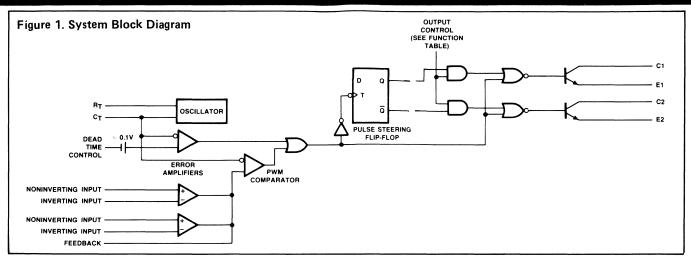
**Test Conditions:**  $V_{CC} = 15V$ ,  $T_A = over recommended operating temperature range, unless otherwise specified.$ 

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
REFEREN	ICE SECTION					
	Output Voltage (Vref)	4.75	5.0	5.25	V	I <sub>O</sub> = 1 mA
	Input Regulation		2.0	25.0	mV	$V_{CC} = 7V$ to $40V$
	Output Regulation		1	15	mV	$I_0 = 1 \text{ to } 10 \text{ mA}$
	Output Voltage Change		0.2	1	%	$\Delta T_A = Min. to Max.$
	with Temperature					
	Short Circuit Output Current	10	35	50	mA	V <sub>ref</sub> = 0 (Note 1) XR-494M only
		_	35	_	mA	V <sub>ref</sub> = 0 (Note 1) XR-494CP and CN
OSCILLA	TOR SECTION				,	
	Frequency		10		kHz	$C_T = 0.01 \mu\text{F}$ , $R_T = 12 \text{k}\Omega$
	Standard Deviation					All values of VCC, CT, RT.
	of Frequency		10		%	T <sub>A</sub> = constant (see Note 2)
	Frequency Change					
	with Voltage		0.1		%	$V_{CC} = 7V \text{ to } 40V, T_A = 25^{\circ}C$
	Frequency Change			2	%	$C_T = 0.01 \mu\text{F}, R_T = 12 \text{k}\Omega$
	with Temperature					$\Delta T_A = Min. to Max.$
DEADTIM	E CONTROL SECTION					
	Input Bias Current (Pin 4)		-2	-10	$\mu \land$	$V_{ } = 0V \text{ to } 5.25V$
	Maximum Duty Cycle					
	(each output)	45			%	$V_I = 0 \text{ (Pin 4)}$
	Input Threshold Voltage	0			V	Maximum Duty Cycle
	(Pin 4)		3	3.3	\ \ \	Zero Duty Cycle
ERROR A	MPLIFIER SECTIONS					
	Input Offset Voltage		2	10	mV	V <sub>O</sub> (Pin 3) = 2.5V
	Input Offset Current		25	250	nA	V <sub>O</sub> (Pin 3) = 2.5V
	Input Bias Current		0.2	1	$\mu \triangle$	$V_0$ (Pin 3) = 2.5V
	Common-Mode Input	-0.3 to				
	Voltage Range	Vcc-2			V	$V_{CC} = 7V$ to $40V$
	Open-Loop Voltage					
	Amplification	70	95		dB	$\Delta V_0 = 3V$ , $V_0 = 0.5V$ to 3.5V
	Unity Gain Bandwidth		800		kHz	
	Common-Mode Rejection Ratio	65	80		dB	$V_{CC} = 40V$ , $T_{A} = 25^{\circ}C$
	Output Sink Current (Pin 3)	0.3	0.7		mA	$V_{ID} = -15 \text{mV} \text{ to } -5 \text{V},$
						V (Pin 3) = 0.7V
	Output Source Current (Pin 3)	-2			mA	$V_{ID} = 15 \text{ mV to 5V, V (Pin 3)} = 3.5V$
OUTPUT S					•	
	Collector Off-State Current		2	100	$\mu \land$	V <sub>CE</sub> = 40V, V <sub>CC</sub> = 40V
	Emitter Off-State Current			-100	$\mu A$	$V_{CC} - V_{C} = 40V, V_{E} = 0$
						$XR-494M Max. = -150 \mu A$
	Collector-Emitter Saturation Volt	age	1.1	1.3	\ \ \	$V_E = 0$ , $I_C = 200 \text{ mA}$
	(Common Emitter)					XR-494M Max. = 1.5V
	(Emitter-Follower)		1.5	2.5	V	$V_C = 15V$ , $I_E = -200 \text{ mA}$
	Output Control Input Current			3.5	mA	$V_I = V_{ref}$
PWM COM	PARATOR SECTION					
	Input Threshold Voltage (Pin 3)		4	4.5	V	Zero Duty Cycle
	Input Sink Current (Pin 3)	0.3	0.7		mA	V (Pin 3) = 0.7V
TOTALDE						
	Standby Supply Current		6	10	mA	V <sub>CC</sub> = 15V Pin 6 at V <sub>ref</sub>
			9	15	mA	V <sub>CC</sub> = 40V All Other Inputs
						and Outputs Open.
	Average Supply Current	1 (	7.5		mA	V = 2V (Pin 4)

Note 1: Duration of the short circuit should not exceed one second.

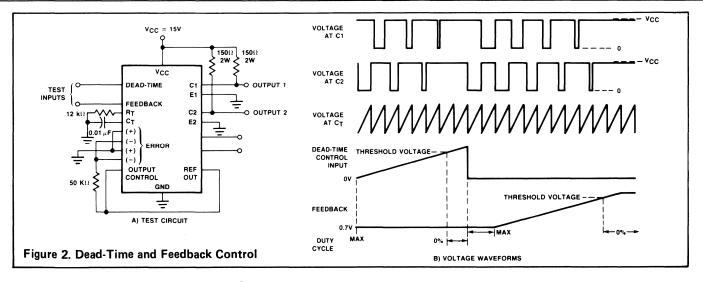
Note 2: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula  $\sigma = 1$ .





#### RECOMMENDED OPERATING CONDITIONS

DADAMETEDO	XR-	494M	1	94CN 194CP	HAUTO
PARAMETERS	MIN	MAX	MIN	MAX	UNITS
Supply Voltage, VCC	7	40	7	40	V
Amplifier Input Voltage, V	-0.3	Vcc-2	03	V <sub>CC</sub> -2	V
Collector Output Voltage, VO		40		40	\ \ \
Collector Output Current (each transistor)		200		200	mA
Current Into Feedback Terminal		0.3		0.3	mA
Timing Capacitor, CT	0.47	10,000	0.47	10,000	nF
Timing Resistor, RT	1.8	500	1.8	500	kΩ
Oscillator Frequency	1	300	1	300	kHz
Operating Free-air Temperature, TA	-55	125	0	75	°C



**SWITCHING CHARACTERISTICS:**  $T_A = 25^{\circ}C$ ,  $V_{CC} = 15V$ .

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Output Voltage Rise Time Output Voltage Fall Time	<u> </u>	100 25	200 100	ns ns	Common-Emitter Configuration (See Figure 4)
Output Voltage Rise Time Output Voltage Fall Time	- -	100 40	200 100	ns ns	Emitter-Follower Configuration (See Figure 5)



#### **FUNCTION TABLE**

INPUTS	OUTPUT FUNCTION	
OUTPUT CONTROL	OUTPUT FUNCTION	
Grounded At V <sub>ref</sub> At V <sub>ref</sub>	Single-ended or parallel output Normal push-pull operation PWM Output at Q1	
At V <sub>ref</sub>	PWM Output at Q2	

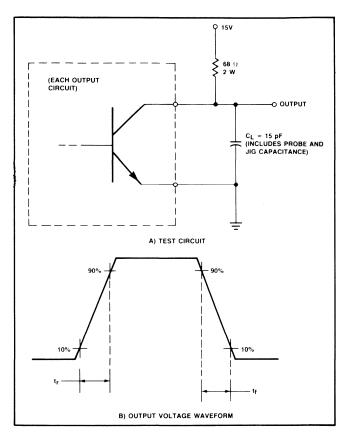


Figure 4. Common Emitter Configuration

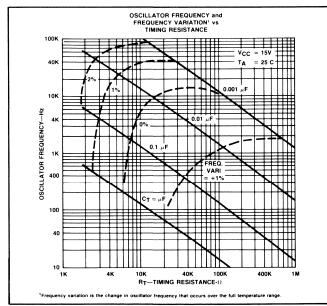


Figure 6. Oscillator Frequency

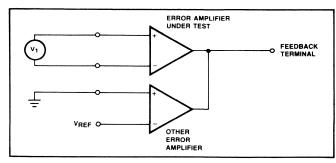


Figure 3. Error-Amplifier Characteristics

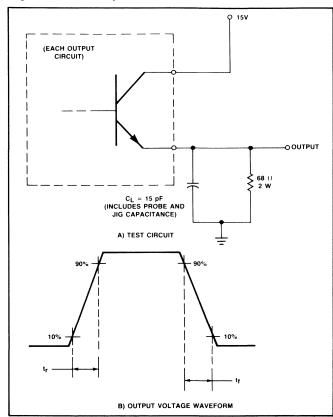


Figure 5. Emitter Follower Configuration

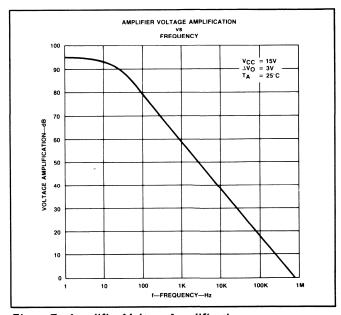


Figure 7. Amplifier Voltage Amplification



## Pulse-Width Modulating Regulator

#### **GENERAL DESCRIPTION**

All functions required to construct a pulse-width modulating regulator are incorporated on a single monolithic chip. The device is primarily designed for power supply control and contains an on-chip 5-volt regulator, two error amplifiers, an adjustable oscillator, a dead-time control comparator, a pulse-steering flip-flop, and output control circuits. Either common emitter or emitter follower output capability is provided by the uncommitted output transistors. Single-ended or push-pull output operation may be selected through the output control function.

The XR-495 also contains an on-chip 39-volt Zener diode for high-voltage applications, where VCC is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

#### **FEATURES**

Complete PWM Power Control Circuitry
Uncommitted Outputs
for 200-mA Sink or Source
Single-ended or Push-pull Operation
Internal Circuitry Prohibits Double Pulse
at Either Output
Variable Dead-time
Current Limiting

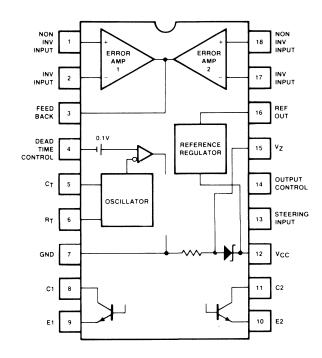
#### **APPLICATIONS**

Power Control Systems Switching Regulators

#### **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, VCC	41 V
Collector Output Voltage	41 V
Amplifier Input Voltage	VCC +0.3V
Collector Output Current	250 mA/each
Power Dissipation 25°C	
Ceramic Package	1000 mW
Derate Above +25°C	8 mW/ <sup>π</sup> C
Plastic Package	625 mW
Derate Above +25°C	5.0 mW/ $^{\pi}$ C
Operating Junction Temperature, TJ	150°C
Storage Temperature	- 65°C to +150°C

#### FUNCTIONAL BLOCK DIAGRAM



#### ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-495M	Ceramic	-55°C to +125°C
XR-495CN	Ceramic	$0^{\circ}$ C to $+70^{\circ}$ C
XR-495CP	Plastic	$0^{\circ}$ C to $+70^{\circ}$ C

#### SYSTEM DESCRIPTION

The XR-495 pulse-width modulator contains all the necessary control functions for a high-performance switching regulator. The XR-495 can be used in step-down, step-up, and inverting configuration, as well as transformer-coupled flyback and push-pull modes with a minimum number of components. Current limiting is possible by using either error amplifier provided on the XR-495. Soft-start function can be achieved by connecting an RC network between the  $V_{\mbox{ref}}$  and the dead-time control pins. The dead-time pin can also be used for over-voltage protection by using a shunt regulator. The output control input must be grounded for single-ended output operation (both inputs tied in parallel). For push-pull configuration, this pin must be tied to the internal 5V reference. Multiple units can be easily synchronized to an external source by providing a sawtooth waveform to the CT terminals, and by terminating the RT pin to the reference output.



#### **ELECTRICAL CHARACTERISTICS**

Test Conditions: VCC = 15V, TA = over recommended operating temperature range, unless otherwise specified.

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
REFEREN	ICE SECTION			<u> </u>		
	Output Voltage (V <sub>ref</sub> )	4.75	5.0	5.25	V	I <sub>O</sub> = 1 mA
	Input Regulation		2.0	25.0	mV -	$V_{CC} = 7V$ to $40V$
	Output Regulation		1	15	mV	$I_0 = 1 \text{ to } 10 \text{ mA}$
	Output Voltage Change		0.2	1	%	$\Delta T_{\Delta}$ = Min. to Max.
	with Temperature					
	Short Circuit Output Current	10	35	50	mA	$V_{ref} = 0$ (Note 1) XR-495M only
			35		mA	V <sub>ref</sub> = 0 (Note 1) XR-495CP and CN
OSCILLA <sup>-</sup>	TOR SECTION					
	Frequency		10		kHz	$C_T = 0.01 \mu\text{F}$ , $R_T = 12 \text{k}\Omega$
	Standard Deviation					All values of VCC, CT, RT.
	of Frequency		10		%	TA = constant (see Note 2)
	Frequency Change					
	with Voltage		0.1		%	$V_{CC} = 7V$ to 40V, $T_A = 25$ °C
	Frequency Change			2	%	$C_{T} = 0.01 \mu\text{F}, R_{T} = 12 k\Omega$
	with Temperature					$\Delta T_{A}$ = Min. to Max.
DEADTIM	IE CONTROL SECTION					
	Input Bias Current (Pin 4)		-2	-10	μΑ	V <sub>I</sub> = 0V to 5.25V
	Maximum Duty Cycle (each output)	45			%	\\\ = 0 \( \mathre{Pin A} \)
	Input Threshold Voltage	0 43			V %	V <sub>I</sub> = 0 (Pin 4) Maximum Duty Cycle
	(Pin 4)		3	3.3	V	Minimum Duty Cycle  Minimum Duty Cycle
	(11114)		3	3.5	V	Willimum Duty Cycle
ERROR A	MPLIFIER SECTIONS					
	Input Offset Voltage		2	10	mV	V <sub>O</sub> (Pin 3) = 2.5V
	Input Offset Current		25	250	nΑ	$V_{O}$ (Pin 3) = 2.5V
	Input Bias Current		0.2	1	$\mu$ A	$V_{O}$ (Pin 3) = 2.5V
	Common-Mode Input	-0.3 to			.,	7.4
	Voltage Range	V <sub>CC</sub> -2			V	$V_{CC} = 7V$ to $40V$
	Open-Loop Voltage	70	O.E.		-10	A)/- 2)/ )/ 0.5)/ 0.5)/
	Amplification	1 /0	95		dB	$\Delta V_0 = 3V$ , $V_0 = 0.5V$ to 3.5V
	Unity Gain Bandwidth Common-Mode Rejection Ratio	GE	800 80		kHz	10V T 05°0
	Output Sink Current (Pin 3)	65 0.3			dB	$V_{CC} = 40V$ , $T_A = 25^{\circ}C$
	Output Sink Current (Fin 5)	0.3	0.7		mA	$V_{ID} = -15 \text{ mV to } -5V,$
	Output Source Current (Pin 3)	-2			^	V (Pin 3) = 0.7V
	Output Source Current (Fin 3)				mA	$V_{1D} = 15 \text{ mV to 5V}, V \text{ (Pin 3)} = 3.5V$
OUTPUT S				T	T	
	Collector Off-State Current		2	100	$\mu$ A	V <sub>CE</sub> = 40V, V <sub>CC</sub> = 40V
	Emitter Off-State Current			-100	$\mu A$	$V_{CC} = V_{C} = 40V$ , $V_{E} = 0$
						$XR-495M \text{ Max.} = -150 \mu\text{A}$
	Collector-Emitter Saturation Volt	age	1.1	1.3	V	VE = 0, I <sub>C</sub> = 200 mA
	(Common Emitter)					XR-495M Max. = 1.5V
	(Emitter-Follower)		1.5	2.5	V	$V_C = 15V$ , $I_E = -200 \text{ mA}$
	Output Control Input Current			3.5	mA	$V_I = V_{ref}$
PWM CON	1PARATOR SECTION					
	Input Threshold Voltage (Pin 3)		4	4.5	V	Zero Duty Cycle
	Input Sink Current (Pin 3)	0.3	0.7		mA	V (Pin 3) = 0.7V
TOTAL DE	EVICE	<b>_</b>	L	l		
	Standby Supply Current		6	10	mA	VCC = 15V Pin 6 at V <sub>ref</sub>
			9	15	mA	$V_{CC} = 40V$ All Other Inputs
			-			and Outputs Open.
	Average Supply Current		7.5		mA	V = 2V (Pin 4)
		<u> </u>		 25	L	



#### **ELECTRICAL CHARACTERISTICS (Continued)**

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
STEERING CONTROL SECTION						
	Input Current			-200 200	=A =A	$V_1 = 0.4V$ $V_1 = 2.4V$
ZENER DIODE SECTION						
	Breakdown Voltage Sink Current		39 0.3		mA	V <sub>CC</sub> = 41V, I <sub>Z</sub> = 2 mA V <sub>I</sub> (Pin 15) = 1V

Note 1: Duration of the short circuit should not exceed one second.

Note 2: Standard deviation is a measure of the statistical distribution about the mean as derived from the formula,  $\sigma = 1$ .

#### **SWITCHING CHARACTERISTICS:** $T_A = 25^{\circ}C$ , $V_{CC} = 15V$ .

PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Output Voltage Rise Time	-	100	200	ns	Common-Emitter Configuration
Output Voltage Fall Time		25	100	ns	(See Figure 4)
Output Voltage Rise Time	<u> </u>	100	200	ns	Emitter-Follower Configuration
Output Voltage Fall Time		40	100	ns	(See Figure 5)

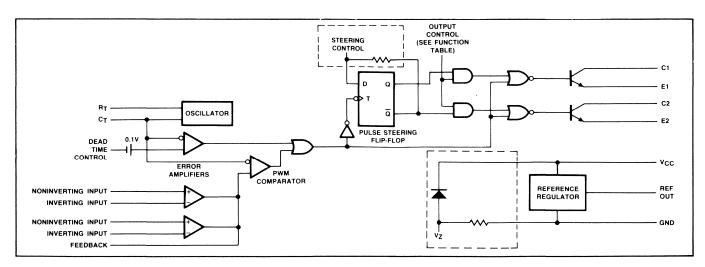


Figure 1. System Block Diagram



IN	PUTS	
OUTPUT CONTROL (Pin 14)	STEERING INPUT (Pin 13)	OUTPUT FUNCTION
Grounded	Open	Single-ended or Parellel Output
Vref	Open	Normal Push-pull Output
Vref V <sub>I</sub> < 0.4V		PWM Output at Q <sub>1</sub>
Vref	$V_1 > 2.4V$	PWM Output at Q <sub>2</sub>

Table 1: Function Table for Output Control.

#### **RECOMMENDED OPERATING CONDITIONS**

PARAMETERS	XF	R-495M	XR XR	UNIT	
FANAMETERS	MIN	MAX	MIN	MAX	UNII
Supply Voltage, VCC	7	40	7	40	V
Amplifier Input Voltages, V <sub>I</sub>	-0.3	V <sub>CC</sub> - 2	-0.3	VCC - 2	V
Collector Output Voltage, VO		40		40	V
Collector Output Current (each transistor)		200		200	mΑ
Current into Feedback Terminal		0.3		0.3	mΑ
Timing Capacitor, C <sub>T</sub>	0.47	10,000	0.47	10,000	nF
Timing Resistor, RT	1.8	500	1.8	500	kΩ
Oscillator Frequency	1	300	1	300	kHz
Operating Free-air Temperature, Тд	-55	125	0	75	°C

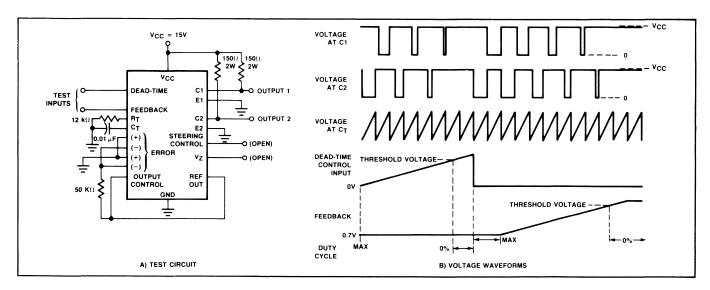


Figure 2: Dead-time and Feedback Control



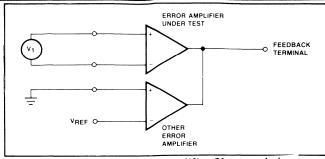


Figure 3: Error Amplifier Characteristics

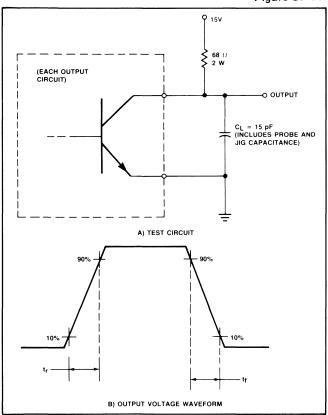


Figure 4. Common-emitter Configuration

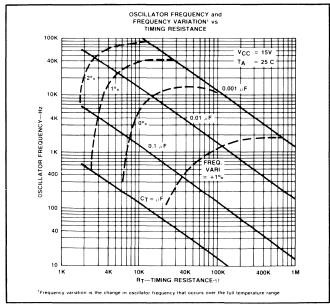


Figure 6: Oscillator Frequency and Frequency Variation vs. Timing Resistance.

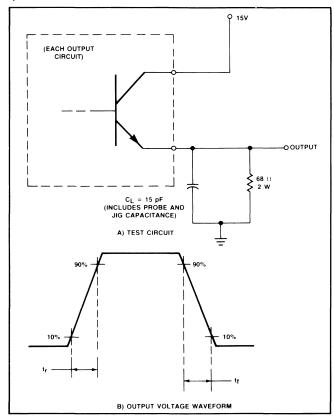


Figure 5: Emitter-follower Configuration

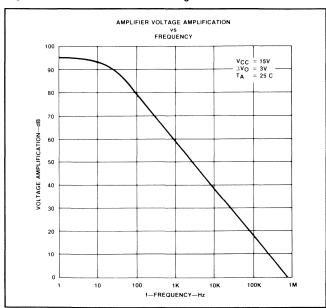


Figure 7. Amplifier Voltage Amplification vs. Frequency.



## **Dual-Polarity Tracking Voltage Regulator**

#### **GENERAL DESCRIPTION**

The XR-1468/1568 is a dual-polarity tracking voltage regulator, internally trimmed for symmetrical positive and negative 15V outputs. Current output capability is 100 mA, and may be increased by adding external pass transistors. The device is intended for local "on-card" regulation, which eliminates the distribution problems associated with single point regulation.

The XR-1468CN and XR-1568N are guaranteed over the  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$  commercial temperature range. The XR-1568M is rated over the full military temperature range of -55°C to +125°C.

#### **FEATURES**

Internally Set for ±15V Outputs ±100 mA Peak Output Current Output Voltages Balanced Within 1% (XR-1568) 0.06% Line and Load Regulation Low-Standby Current Output Externally Adjustable from ±14.5 to ±20 Volts Externally Adjustable Current Limiting Remote Sensing

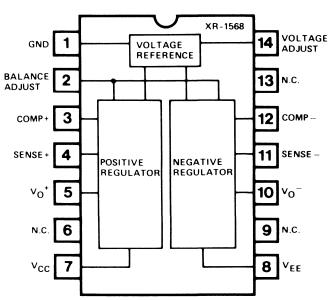
#### **APPLICATIONS**

Main Regulation in Small Instruments On-Card Regulation in Analog and Digital Systems Point-of-Load Precision Regulation

#### **ABSOLUTE MAXIMUM RATINGS**

Power Supply Minimum Short-Circuit Resistance Load Current, Peak	±30 Volts 4.0 Ohms ±100 mA
Power Dissipation Ceramic (N) Package	1.0 Watt
Derate Above +25°C	6.7 mW/°C
Operating Temperature XR-1568M XR-1468C/1568 Storage Temperature	-55°C to +125°C 0°C to +70°C -65°C to +150°C

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Part Number	Package	Operating Temperature
XR-1568M	Ceramic	-55°C to +125°C
XR-1568N	Ceramic	0°C to +70°C
XR-1468CN	Ceramic	$0^{\circ}$ C to $+70^{\circ}$ C

#### SYSTEM DESCRIPTION

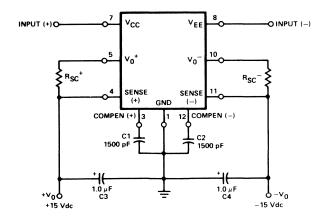
The XR-1468/1568 is a dual polarity tracking voltage regulator combining two separate regulators with a common reference element in a single monolithic circuit, thus providing a very close balance between the positive and negative output voltages. Outputs are internally set to ±15 volts but can be externally adjusted between ±8.0 to ±20 volts with a single control. The circuit features ±100 mA output current, with externally adjustable current limiting, and provision for remote voltage sensing.



#### **ELECTRICAL CHARACTERISTICS**

Test Conditions:  $V_{CC}$  = +20V,  $V_{EE}$  = -20V, C1 = C2 = 1500 pF, C3 = C4 = 1.0  $\mu$ F, R<sub>SC</sub>+ = R<sub>SC</sub>- = 4.0  $\Omega$ .  $I_{L}$ + =  $I_{L}$ - = 0,  $I_{C}$  = +25°C unless otherwise noted. See Figure 1.

DADAMETER		XR-1468C XR-1568				HALLT	CONDITIONS	
PARAMETER -	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Output Voltage	14.5	15	15.5	14.8	15	15.2	Vdc	
Input Voltage			30			30	Vdc	
Input-Output Voltage Differential	2.0			2.0			Vdc	
Output Voltage Balance		±50	±300		±50	±150	mV	
Line Regulation Voltage			10 20			10 20	mV	V <sub>in</sub> = 18V to 30V T <sub>L</sub> to T <sub>H</sub>
Load Regulation Voltage			10			10	mV	IL = 0 to 50 mA, TJ = constant
			30			30		TA = TL to TH
Output Voltage Range	8.0		20	8.0		20	Vdc	See Figure 1
Ripple Rejection		75			75		dB	f = 120 Hz
Output Voltage Temperature Stability		0.3	1.0		0.3	1.0	%	T <sub>L</sub> to T <sub>H</sub>
Short-Circuit Current Limit		60			60		mA	RSC = 10 ohms
Output Noise Voltage		100			100		<b>μ</b> ∨rms	BW = 10 Hz - 10 kF
Positive Standby Current		2.4	4.0		2.4	4.0	mA	V <sub>in</sub> = +30V
Negative Standby Current		1.0	3.0	-	1.0	3.0	mA	V <sub>in</sub> = -30V
Long-Term Stability		0.2			0.2		%/kHr	



C1 and C2 should be located as close to the device as possible. A 0.1  $\mu F$  ceramic capacitor may be required on the input lines if the device is located an appreciable distance from the rectifier filter capacitors.

Figure 1. Basic 50 mA Regulator

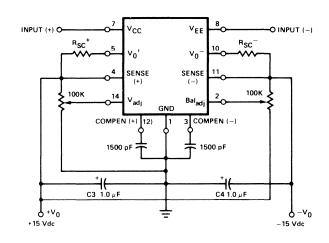


Figure 2. Voltage Adjust and Balance Adjust Circuit

C3 and C4 may be increased to improve load transient response and to reduce the output noise. It is low temperature operation, it may be necessary to bypass C4 with a 0.1  $\mu$ F coramic disc capacitor.



## Pulse-Width Modulating Regulator

#### **GENERAL DESCRIPTION**

The XR-1524 family of monolithic integrated circuits contain all the control circuitry for a switching regulator power supply. Included in a 16-Pin dual-in-line package is the voltage reference, an error amplifier, an oscillator, a pulse-width modulator, a pulse-steering flip-flop, dual alternating output switches and current limiting, and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled dc to dc converters, transformerless voltage doublers, and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C, while the XR-2524/3524 are designed for commercial applications of 0°C to +70°C.

#### **FEATURES**

Direct Replacement for SG-1524/2524/3524 Complete PWM Power Control Circuitry Single-ended or Push-pull Outputs Line and Load Regulation of 0.2% 1% Maximum Temperature Variation Total Supply Current Less Than 10 mA Operation Beyond 100 kHz

#### **APPLICATIONS**

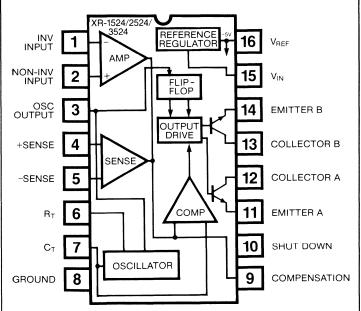
Storage Temperature

Switching Regulators
Pulse-Width Modulated Power Control Systems

#### **ABSOLUTE MAXIMUM RATINGS**

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate Above +25°C	8 mW/°C
Plastic Package	625 mW
Derate Above +25°C	5.0 mW/°C
Operating Temperature	
XR-1524	-55°C to +125°C
XR-2524/3524	0°C to +70°C

#### **FUNCTIONAL BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Part Number	Package	Operating Temperature
XR-1524M	Ceramic	-55°C to +125°C
XR-2524N	Ceramic	0°C to +70°C
XR-2524P	Plastic	0°C to + 70°C
XR-3524N	Ceramic	0°C to +70°C
XR-3524P	Plastic	0°C to +70°C

#### SYSTEM DESCRIPTION

The XR-1524 series of pulse-width modulating control circuits can be used in step-up, step-down, and inverting types of switching regulators. It is capable of maintaining an output from input voltages between 8 and 40 volts. By connecting Pin 15 and Pin 16 together, it can be operated from a fixed 5-volt supply. The output drivers can handle over 50 mA of current, and can be used in a push-pull configuration or a single-ended mode. A simple soft-start circuit, which is made up of a diode and an RC network, keeps the output drivers off when power is first applied to the device. As the capacitor charges up, the duty cycle is slowly increased, causing the output drivers to slowly turn on.

-65°C to +150°C





#### **ELECTRICAL CHARACTERISTICS**

Test Conditions:  $T_A = -55^{\circ} \text{C}$  to +125°C for the XR-1524, and 0°C to +70°C for the XR-2524/3524,  $V_{\text{IN}} = 20 \text{V}$ , and f = 20 kHz, unless otherwise specified.

	Х	R-1524/2	524		XR-3524		115117		
PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
REFERENCE SECTION Output Voltage Line Regulation Load Regulation Ripple Rejection	4.8	5.0 10 20 66	5.2 20 50	4.6	5.0 10 20 66	5.4 30 50	V mV mV dB	V <sub>IN</sub> = 8 to 40V I <sub>L</sub> = 0 to 20 mA f = 120 Hz, T <sub>A</sub> = 25°C	
Short Circuit Current Limit Temperature Stability Long Term Stability		100 0.3 20	1 .		100 0.3 20	1	mA % mV/khr	V <sub>ref</sub> = 0, T <sub>A</sub> = 25°C Over Operating Temp. Range T <sub>A</sub> = 25°C	
OSCILLATOR SECTION Maximum Frequency Initial Accuracy Voltage Stability Temperature Stability Output Amplitude Output Pulse Width		300 5 3.5 0.5	1 2		300 5 3.5 0.5	1 2	kHz % % V <b>μ</b> s	$C_T = .001  \mu F$ , $R_T = 2  k \Omega$ , $R_T$ and $C_T$ constant $V_{IN} = 8$ to $40V$ , $T_A = 25^{\circ}C$ , Over Operating Temp. Range Pin 3, $T_A = 25^{\circ}C$ $C_T = .01  \mu F$ , $T_A = 25^{\circ}C$	
ERROR AMPLIFIER SECTIO Input Offset Voltage Input Bias Current Open-Loop Voltage Gain Common-Mode Voltage	72 1.8	0.5 2 80	5 10 3.4	60 1.8	2 2 80	10 10 3.4	mV μA dB V	$V_{CM} = 2.5V$ $V_{CM} = 2.5V$ $T_{A} = 25^{\circ}C$	
Common-Mode Rejection Ratio Small Signal Bandwidth Output Voltage	0.5	70	3.8	0.5	70 3	3.8	dB MHz V	$T_A = 25^{\circ}C$ $A_V = 0 \text{ dB, } T_A = 25^{\circ}C$ $T_A = 25^{\circ}C$	
COMPARATOR SECTION  Duty Cycle Input Threshold Input Threshold Input Bias Current	0	1 3.5 1	45	0	1 3.5 1	45	% ∨ ∨ μΑ	% Each Output On Zero Duty Cycle Max. Duty Cycle	
CURRENT LIMITING SECTION Sense Voltage  Sense Voltage Temp. Coef.	DN 190	200	210	180	200	220	mV mV/°C	Pin 9 = 2V with Error Amplifier, Set for Max. Out, $T_A = 25^{\circ}C$	
Common-Mode Voltage OUTPUT SECTION (Each Out Max. Collector- Emitter Voltage Collector Leakage Current Saturation Voltage Emitter Output Voltage Rise Time Fall Time	-1 put) 40 17	0.1 1 18 0.2 0.1	50 2	40	0.1 1 18 0.2 0.1	50 2	∨ μΑ ∨ ν μs μs	$V_{CE} = 40V$ $I_{C} = 50 \text{ mA}$ $V_{IN} = 20V$ $R_{C} = 2 \text{ k}\Omega$ , $T_{A} = 25^{\circ}\text{C}$ $R_{C} = 2 \text{ k}\Omega$ , $T_{A} = 25^{\circ}\text{C}$	
TOTAL STANDBY CURREN (Excluding oscillator charging current error and current limit dividers, and with outputs open.)	Г	8	10		8	10	mA	V <sub>IN</sub> = 40V	



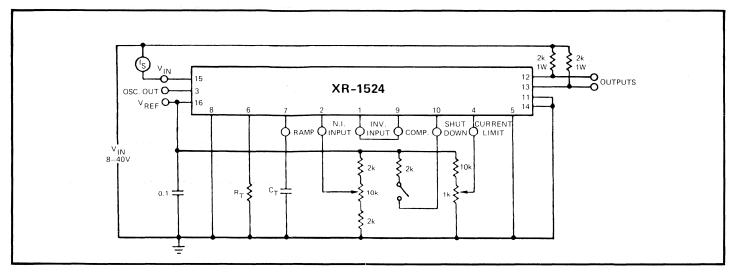


Figure 1: Open Loop Test Circuit.

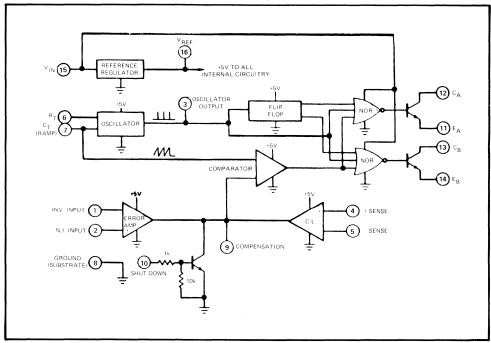


Figure 2: Detailed System Block Diagram of XR-1524.

#### PRINCIPLES OF OPERATION

#### Voltage Reference Section

The internal voltage reference and regulator section provvides a 5-volt reference output at Pin 16. This voltage also serves as a regulated voltage source for the internal timing and control circuitry. This regulator may be bypassed for operation from a fixed 5-volt supply by connecting Pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5-volt source for other circuitry. It will provide up to 50 mA of current itself, and can easily be expanded to higher currents with an external pnp as shown in Figure 3.

#### **Oscillator Section**

The oscillator section in the XR-1524 uses an external resistor (RT) to establish a constant charging current into an external capacitor (CT). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The charging current is equal to 3.6V÷ RT and should be kept within the range of approximately 30  $\mu\text{A}$  to 2 mA, i.e., 1.8K < RT < 100K.

The oscillator period is approximately  $T = R_T C_T$ , where T is in microseconds when  $R_T$  = ohms, and  $C_T$  = microfarads.



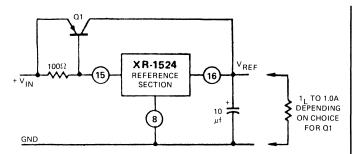


Figure 3: Using the Internal Regulator as 5V Power Supply for External Circuitry.

The use of Figure 4 allows the selection of  $R_T$  and  $C_T$  for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0 – 90% duty cycle, and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each output's duty cycle is 0 – 45%, and the overall frequency is 1/2 that of the oscillator.

The range of values for CT also has limits as the discharge time of CT determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead-time relationship is shown in Figure 5. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flop's reaching a stable state. If small values of CT must be used, the pulse width may still be expanded by adding a shunt capacitance ( $\approx$  100 pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of CT fall between .001 and 0.1  $\mu$ F.

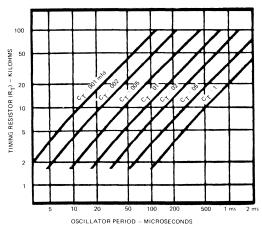


Figure 4: Oscillator Period as a Function of RT and CT.

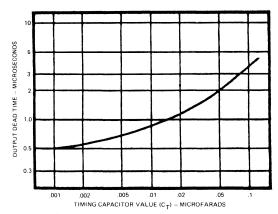


Figure 5: Output State Dead-time as a Function of the Timing Capacitor Value.

If it is desired to synchronize the XR-1524 to an external clock, a pulse of  $\approx$  + 3 volts may be applied to the oscillator output terminal with R<sub>T</sub>C<sub>T</sub> set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2 kM.

If two or more XR-1524 circuits must be synchronized together, one must be designated as master with its R $_{T}$ C $_{T}$  set for the correct period. The slaves should each have an R $_{T}$ C $_{T}$ , set for approximately 10% longer period than the master; with the added requirement that C $_{T}$  (slave) = 1/2 C $_{T}$  (master). Then connecting Pin 3 on all units together will insure that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

#### **Error Amplifier Section**

The error amplifier is a simple differential-input, transconductance amplifier. The output is the compensation terminal, Pin 9, which is a high-impedance node (R<sub>L</sub>  $\approx$  5 m $\Omega$ ). The gain is:

 $A_V = g_m R_L = \frac{8 I_C R_L}{2kT} \approx .002 R_L$ 

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from Pin 9 to ground, as shown in Figure 6.

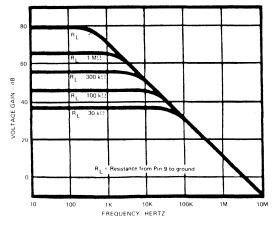


Figure 6: Error Amplifier Frequency Response as a Function of External Resistor, RL, at Pin 9.





In addition to dc gain control, the compensation terminal is also the place for ac phase compensation. The frequency response curves of Figure 6 show the uncompensated amplifier with a single pole at approximately 200 Hz, and a unity gain cross-over at 5 MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series RC combination between Pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50 k $\Omega$  plus .001  $\mu$ F.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200  $\mu\mathrm{A}$  can pull this point to ground, thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback, and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5-volt reference voltage must be divided down as shown in Figure 7. The error amplifier may also be used in fixed duty cycle applications by using the unit gain configuration shown in the open loop test circuit.

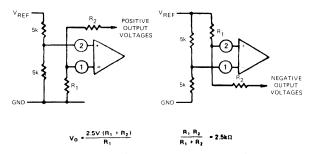


Figure 7: Error Amplifier Biasing Circuits.

(Note: Change in Input Connections for Opposite Polarity Outputs.)

#### **Current Limiting Controls**

The current limiting circuitry of the XR-1524 is shown in Figure 8.

By matching the base-emitter voltages of  $Q_1$  and  $Q_2$ , and assuming negligible voltage drop across  $R_1$ ,

Threshold =  $V_{BE}$  (Q<sub>1</sub>) +  $I_1R_2$  -  $V_{BE}$  (Q<sub>2</sub>) =  $I_1R_2$  $\approx 200 \text{ mV}$  Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use. The most important of which is the  $\pm$  1 volt common-mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R<sub>1</sub>C<sub>1</sub> and Q<sub>1</sub> provides a rolloff pole at approximately 300 Hz.

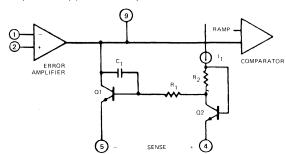


Figure 8: Current Limiting Circuitry of the XR-1524.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, Pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 16.) Another application is to ground Pin 5 and use Pin 4 as an additional shutdown terminal, i.e., the output will be off with Pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 9. This circuit can reduce the short-circuit current (ISC) to approximately 1/3 the maximum available output current (IMAX).

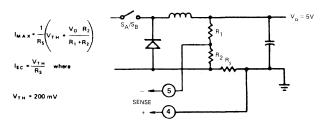


Figure 9: Foldback Current Limiting Used to Reduce Power Dissipation Under Shorted Output Conditions.

#### **Output Circuits**

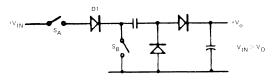
The outputs of the XR-1524 are two identical npn transistors, with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry for fast response, and current limiting set for a maximum output current of approximately 100 mA. The availability of both collectors and emitters allows maximum versatility to enable driving either npn or pnp external transistors.

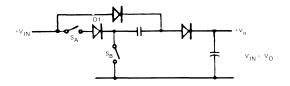


In considering the application of the XR-1524 for voltage regulator circuitry, there are a multitude of output configurations possible. In general, however, they fall into three basic classifications:

- 1. Capacitor-diode coupled voltage multipliers.
- 2. Inductor-capacitor single-ended circuits
- 3. Transformer-coupled circuits.

Examples of each category are shown in Figure 10, 11, and 12. In each case, the switches indicated can be either the output transistors in the XR-1524 or added external transistors according to the load current requirements.





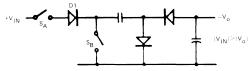
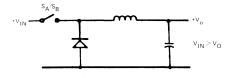
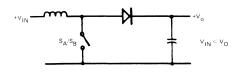


Figure 10: Capacitor-Diode Coupled Voltage Multiplier
Output Stages. (Note: Diode D<sub>1</sub> is necessary
to Prevent Reverse Emitter-Base Breakdown
of Transistor Switch, S<sub>A</sub>.)





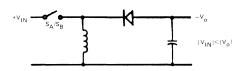


Figure 11: Single-ended Inductor Circuits Where the Two Outputs of the XR-1524 are Connected in Parallel.

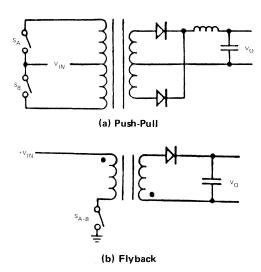


Figure 12: Push-Pull and Flyback Connections for Transformer-Coupled Outputs.

#### **Deadband Control**

The XR-1524 pulse-width modulating regulator provides two outputs which alternate in turning on for push-pull inverter applications. The internal oscillator sends a momentary blanking pulse to both outputs at the end of each period to provide a deadband so that there cannot be a condition when both outputs are on at the same time. The amount of deadband is determined by the width of the blanking pulse appearing on Pin 3, and can be controlled by any one of the four techniques described below:

Method 1: For 0.2 to 2.0 microseconds, the deadband is controlled by the timing capacitor,  $C_T$ , on Pin 7. The relationship between  $C_T$  and deadband is shown in Figure 5. Of course, since  $C_T$  also helps determine the operating frequency, the range of control is somewhat limited.

Method 2: For 0.5 to 5.0 microseconds, the blanking pulse may be extended by adding a small capacitor from Pin 3 to ground. The value of the capacitor must be less than 1000 pF or triggering will become unreliable.

Method 3: For longer and more well-controlled blanking pulses, a simple one-shot latch similar to the circuit shown in Figure 13 should be used.

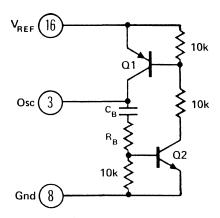
When this circuit is triggered by the oscillator output pulse, it will latch for a period determined by CBRB providing a well-defined deadband.

Another use for this circuit is as a buffer when several other circuits are to be synchronized to one master oscillator. This one-shot latch will provide an adequate signal to insure that all the slave circuits are completely reset before allowing the next timing period to begin.





Note that with this circuit, the blanking pulse holds off the oscillator so its width must be subtracted from the overall period when selecting  $R_{\rm T}$  and  $C_{\rm T}.$ 



Q1 and Q2 = Small Signal General Purpose Transistors

Figure 13: Recommended External Circuitry for Long Duration Blanking Pulse Generation, (Method 3 of Deadband Control. Note: For 5  $\mu$ sec blanking, choose C<sub>B</sub> = 200 pF, R<sub>B</sub> = 10  $\pi$ M.)

Method 4: Another way of providing greater deadband is just to limit the maximum pulse width. This can be done by using a clamp to limit the output voltage from the error amplifier. A simple way of achieving this clamp is with the circuit shown in Figure 14.

This circuit will limit the error amplifiers voltage range, since its current source otuput will only supply 200  $\mu$ A. Additionally, this circuit will not affect the operating frequency.

AΡ

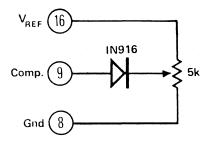


Figure 14: Using a Clamp Diode to Control Deadband (Method 4 of Deadband Control).

#### APPLICATIONS INFORMATION

**Polarity Converting Regulator:** The XR-1524 pulse-width modulating regulator can be interconnected as shown in Figure 15. The component values shown in the figure are chosen to generate a -5-volt regulated supply voltage from a +15-volt input. This circuit is useful for an output current of up to 20 mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

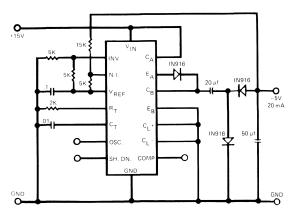


Figure 15: Circuit Connection for Polarity Converting Regulator ( $V_{in} = +15V$ ,  $V_{out} = -5V$ ).

**Flyback Converter:** Figure 16 shows the application of XR-1524 in a low current dc-dc converter, using the flyback converter principle (see Figure 12b). The particular values given in the figure are chosen to generate  $\pm$  15 volts at 20 mA from a +5-volt regulated line. The reference generator in the XR-1524 is unused. The reference is provided by the input voltage. Current limiting in a flyback converter is difficult, and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

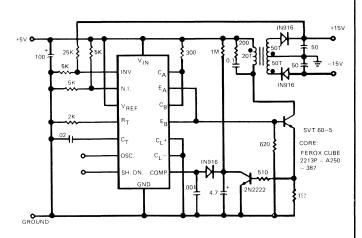


Figure 16: A Low-Current dc-dc Converter Using Flyback Principle.  $(V_{out} = \pm 15V, V_{in} = +5V, I_L \times 20 \text{ mA}).$ 





**Single-ended Regulator:** The XR-1524 operates as an efficient single-ended pulse-width modulating regulator, using the circuit connection shown in Figure 17. In this configuration, the two output transistors of the circuit are connected in parallel by shorting Pins (12,13) and (11,14) together, respectively, to provide for effective 0 – 90% duty cycle modulation. The use of an output inductance requires an RC phase compensation on Pin 9, as shown in the figure.

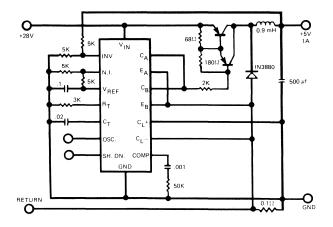


Figure 17: Conventional Single-ended Regulator Connection.  $(V_{in} = +28V, \ V_O = +5V, \ I_{out} \leqslant 1 \ Amp)$ 

**Push-pull Converter:** The circuit of Figure 18 shows the use of the XR-1524 in a transformer-coupled dc-dc converter with push-pull outputs (see Figure 12a). Note that the oscillator must be set at twice the desired output frequency as the XR-1524's internal flip-flop divides the frequency by 2 as it switches the PWM signal from one output to the other. Current limiting is done in the primary. This causes the pulse width to be reduced automatically, if the transformer saturation occurs.

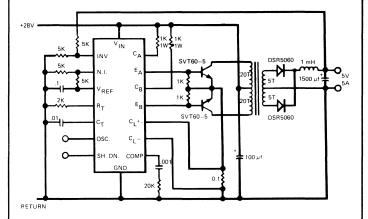


Figure 18: A High-Current dc-dc Converter with Push-pull Outputs.  $(V_{in} = +28V, V_{O} = +5V, I_{O} \le 5A)$ 



# Pulse-Width Modulating Regulators

### **GENERAL DESCRIPTION**

The XR-1525A/1527A is a series of monolithic integrated circuits that contain all of the control circuitry necessary for a pulse-width modulating regulator. Included in the 16-Pin dual-in-line package is a voltage reference, an error amplifier, a pulse-width modulator, an oscillator, undervoltage lockout, soft-start circuitry, and output drivers.

The XR-1525A/2525A/3525A series features NOR logic, giving a LOW output for an OFF state. The XR-1527A/2527A/3527A series features OR logic, giving a HIGH output for an OFF state.

# **FEATURES**

8V to 35V Operation
5.1V Reference Trimmed to ± 1%
100 Hz to 500 kHz Oscillator Range
Separate Oscillator Sync Terminal
Adjustable Deadtime Control
Internal Soft-Start
Input Under-voltage Lockout
Latching PWM to Prevent Double Pulsing
Dual Source/Sink Output Drivers
Capable of Over 200 mA
Power-FET Drive Capability

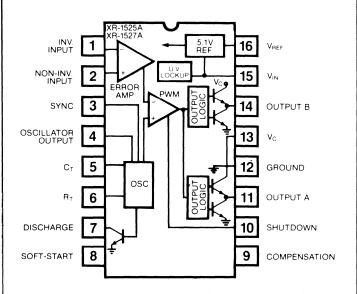
# **APPLICATIONS**

Power Control Systems Switching Regulators Industrial Controls

# **ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (+ V <sub>IN</sub> )	+ 40V
Collector Supply Voltage (V <sub>C</sub> )	+ 40V
Logic Inputs	-0.3V to 5.5V
Analog Inputs	$-0.3V$ to $+V_{1N}$
Output Current, Source or Sink	500 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation	
Ceramic Package	1000 mW
Derate above $T_A = +25^{\circ}C$	8.0 mW/°C
Plastic Package	625 mW
Derate above $T_A = +25^{\circ}C$	5.0 mW/°C
Operating Junction Temperature (T <sub>J</sub> )	+ 150°C
Storage Temperature Range	-65°C to +150°C

# **FUNCTIONAL BLOCK DIAGRAM**



# **ORDERING INFORMATION**

Part Number	Package	Operating Temperature
XR-1525A/27AN	Ceramic	-55°C to +125°C
XR-2525A/27AN	Ceramic	-25°C to +85°C
XR-2525A/27AP	Plastic	-25°C to +85°C
XR-3525A/27AN	Ceramic	0°C to +70°C
XR-3525A/27AP	Plastic	0°C to +70°C

# SYSTEM DESCRIPTION

The on-chip 5.1-volt reference is trimmed to  $\pm$  1% initial accuracy, and the common-mode input range of the error amplifier is extended to include the reference voltage. Deadtime is adjustable with a single external resistor. A sync input to the oscillator allows multiple units to be slaved together, or a single unit to be synchronized to an external clock. A positive-going signal applied to the shutdown pin provides instantaneous turnoff of the outputs. The under-voltage lockout circuitry keeps the output drivers off, and the soft-start capacitor discharged, for an input voltage below the required value. The latch on the PWM comparator insures the outputs to be active only once per oscillator period, thereby eliminating any double pulseing. The latch is reset with each clock pulse.

The output drivers are totem-pole designs capable of sinking and sourcing over 200 mA.



# **ELECTRICAL CHARACTERISTICS**

**Test Conditions:**  $V_{IN} = +20V$ ,  $T_{J} = Full operating temperature range, unless otherwise specified.$ 

DADAMETED	XI XI	R-1525A/25 R-1527A/25	525A 527A	. ;:	XR-3525/ XR-3527/		шыт	CONDITIONS
PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
VOLTAGE REFERENCE SECTION	٧							
Output Voltage Line Regulation Load Regulation Temperature Stability (2) Total Output Variation (2) Output Short	5.05 5.00	5.10 10 20 20	5.15 20 50 50 50 5.20	5.00 4.95	5.10 10 20 20	5.20 20 50 50 5.25	V mV mV V	T <sub>J</sub> = 25°C V <sub>IN</sub> = 8V to 35V I <sub>L</sub> = 0 to 20 mA T <sub>J</sub> = Full Operating Range Line, Load & Temperature
Circuit Current Output Noise Voltage (2) Long Term Stability (2)		80 40 20	100 200 50		80 40 20	100 200 50	mA μV rms mV/kHR	$T_J = 25^{\circ} \text{C}, V_{ref} = 0 \text{V}$ $T_J = 25^{\circ} \text{C}, 10 \text{ Hz} \le f \le 10 \text{ kHz}$ $T_J = 125^{\circ} \text{C}$
OSCILLATOR SECTION (Note 3)								
Initial Accuracy (2,3) Temperature Stability (2) Input Voltage Stability (2,3) Minimum Frequency Maximum Frequency Current Mirror Clock Amplitude (2,3) Clock Pulse Width (2,3) Sync Threshold Sync Input Current	400 1.7 3.0 0.3 1.2	± 2 ± 3 ± 0.3 ± 0.3 2.0 3.5 0.5 2.0 1.0	± 6 ± 6 ± 1 100 2.2 1.0 2.8 2.5	400 1.7 3.0 0.3 1.2	± 2 ± 3 ± 1 2.0 3.5 0.5 2.0 1.0	± 6 ± 6 ± 2 100 2.2 1.0 2.8 2.5	% % Hz kHz mA V µsec V	$T_J = 25^{\circ}C$ , $f = 40$ kHz $T_J = Full$ Operating Range $V_{IN} = 8V$ to $35V$ $R_T = 150$ k $\Omega$ , $C_T = 0.1$ $\mu$ F $R_T = 2$ k $\Omega$ , $C_T = 1$ nF $I_{RT} = 2$ mA $T_J = 25^{\circ}C$ , $R_D = 0\Omega$ Sync Voltage = 3.5V
ERROR AMPLIFIER SECTION (VC	<sub>M</sub> = 5.1V	)						
Input Offset Voltage Input Bias Current Input Offset Current DC Open-Loop Gain Gain Bandwidth Product (2) Output Low Voltage Output High Voltage	60 1 3.8	0.5 1 75 2 0.2 5.6	5.0 10 1	60 1 3.8	2 1 75 2 0.2 5.6	10 10 1	mV μA μA dB MHz V	R <sub>L</sub> > 10 MΩ T <sub>J</sub> = 25°C
Common-Mode Rejection Ratio Supply Voltage Rejection Ratio	60 50	75 60		60 50	75 60		dB dB	$V_{CM} = 1.5V \text{ to } 5.2V$ $V_{IN} = 8V \text{ to } 35V$
PULSE-WIDTH MODULATING COI			L	ш	L	<u> </u>		1 1/14 01 10 001
Minimum Duty Cycle Maximum Duty Cycle Input Threshold (3) Input Threshold (3) Input Bias Current (2)	45 0.6	49 0.9 3.3 0.05	3.6 1.0	45 0.6	49 0.9 3.3 0.05	0 3.6 1.0	% % V V μΑ	Zero Duty Cycle Maximum Duty Cycle
SOFT-START SECTION								
Soft-Start Current Soft-Start Voltage Shutdown Input Current	25	50 0.4 0.4	80 0.6 1.0	25	50 0.4 0.4	80 0.6 1.0	μΑ V mA	V <sub>shutdown</sub> = 0V V <sub>shutdown</sub> = 2V V <sub>shutdown</sub> = 2.5V
OUTPUT DRIVERS (Each Output)	V <sub>C</sub> = 20V							
Output Low Voltage Output Low Voltage Output High Voltage Output High Voltage Under-voltage Lockout Collector Leakage (4) Rise Time (2) Fall Time (2) Shutdown Delay (2)	18 17 6	0.2 1.0 19 18 7 100 50 0.2	0.4 2.0 8 200 600 300 0.5	18 17 6	0.2 1.0 19 18 7 100 50 0.2	0.4 2.0 8 200 600 300 0.5	V V V V μA nsec nsec μsec	I <sub>sink</sub> = 20 mA I <sub>sink</sub> = 100 mA I <sub>source</sub> = 20 mA I <sub>source</sub> = 100 mA V <sub>comp</sub> and V <sub>SS</sub> = High V <sub>C</sub> = 35 V T <sub>J</sub> = 25° C, C <sub>L</sub> = 1 nF T <sub>J</sub> = 25° C, C <sub>L</sub> = 1 nF V <sub>SD</sub> = 3V, C <sub>S</sub> = 0, T <sub>J</sub> = 25° C
TOTAL STANDBY CURRENT								
Supply Current		14	20		14	20	mA	V <sub>IN</sub> = 35V

Note 2: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production. Note 3: Tested at f = 40 kHz (R<sub>T</sub> = 3.6 k $\Omega$ , C<sub>T</sub> = 0.01  $\mu$ F, R<sub>D</sub> = 0 $\Omega$ ). Note 4: Applies to XR-1525A/2525A/3525A only, due to polarity of output pulses.



### PRINCIPLES OF OPERATION

The different control blocks within the XR-1525A/1527A function as follows:

#### Voltage Reference Section

The internal voltage reference circuit of the XR-1525A/1527A is based on the well-known "band-gap" reference, with a nominal output voltage of 5.1 volts, internally trimmed to ± 1% accuracy. It is short circuit protected and is capable of providing up to 20 mA of reference current. A simplified circuit schematic is shown in Figure 7.

#### **Oscillator Section**

The sawtooth oscillator derives its frequency from an external timing resistor/capacitor pair. The timing resistor,  $R_T$ , determines the charging current into the timing capacitor,  $C_T$ . The magnitude of this current is approximately given by:

$$\frac{\text{V}_{\text{ref}} \cdot 2\text{V}_{\text{BE}}}{\text{R}_{\text{T}}} \, \approx \, \frac{3.7\text{V}}{\text{R}_{\text{T}}}$$

where  $R_T$  may range from 2 k $\Omega$  to 150 k $\Omega$ . In general, temperature stability is maximized with lower values of R<sub>T</sub>. The current source charging C<sub>T</sub> creates a linear ramp voltage which is compared to fixed thresholds within. When the capacitor voltage reaches +3.3 volts, the oscillator output (Pin 4) goes high, turning ON the discharge transistor. The capacitor is discharged through the deadtime resistor,  $R_D$ . When the voltage on  $C_T$  falls to +1.0 volt, the oscillator output goes low, the discharge transistor is turned OFF, and the capacitor is charged through the constant current source as another cycle starts. With large values of  $R_D$  (500 $\Omega$ , maximum), deadtime is increased. The actual operating frequency is thus a function of the charge and discharge times. Figure 2 shows how charge time is related to  $R_T$  and  $C_T$ , with  $R_D = 0\Omega$ . Deadtime is a function of  $R_D$  and  $C_T$ , and can vary between 0.5 to 7  $\mu$ sec, with  $R_D = 0\Omega$ , as shown in Figure 3. The equivalent circuit schematic of the oscillator section is shown in Figure 8.

A unit can be synchronized to an external source by selecting its free-running oscillator period to be 10% longer than the period of the external source. A positive-going pulse of at least 300 nsec wide should be applied to the sync terminal for reliable triggering; however, it should not exceed the free-running pulse width by more than 200 nsec. The amplifier of the pulse should be kept between 2 and 5 volts. Multiple units can be synchronized to each other by connecting all  $C_{\mathsf{T}}$  pins, and oscillator output pins together;  $R_{\mathsf{T}}$  pins and discharge pins on slave oscillators must be left open.

# **Error Amplifier**

The error amplifier of the XR-1525A/1527A is a differential input transconductance amplifier. Its common-mode range covers the reference voltage. Its open-loop gain, typically 75 dB, can be reduced by a load resistor on Pin 9. To ensure proper operation, the output load should be limited to 50 k $\Omega$  or greater. An equivalent circuit schematic of the error amplifier is shown in Figure 9.

#### **Soft-Start Circuitry**

The soft-start function is provided to achieve controlled turn-on of the pulse-width modulator. When power is applied to the device, the external capacitor,  $C_{SOft-start}$ , on Pin 8 is charged by a 50  $\mu$ A constant current source. The ramp voltage appearing on this capacitor is fed into the pulse-width modulator, which gradually increases its output duty cycle from zero to the prescribed value. When the shutdown terminal is raised to a positive value, an internal transistor turns ON, and discharges the capacitor,  $C_S$ , causing the PWM to turn OFF. When the shutdown terminal is open or pulled low, the transistor turns OFF, and  $C_S$  begins charging as before. The turn-on time (time required to charge  $C_S$  to +2.7 volts) can be approximated as:

$$T_C$$
 (msec) = 54  $C_S$ 

where  $C_S$  is in  $\mu F$ .

# **Output Section**

The output drivers of the XR-1525A/1527A are totempole designs capable of sinking and sourcing 200 mA. The low source impedance in the high or low states provides ideal interfacing with bipolar as well as FET power transistors. Either push-pull or single-ended output configurations are possible with separate collector supply terminals. The equivalent schematic of the output drivers is shown in Figure 10.

# RECOMMENDED OPERATING CONDITIONS

Note 1: Range over which the device is functional and parameter limits are guaranteed.

Collector Supply Voltage ( $V_C$ ) +4.5V to +35V Sink/Source Load Current (Steady State) 0 to 100 mA



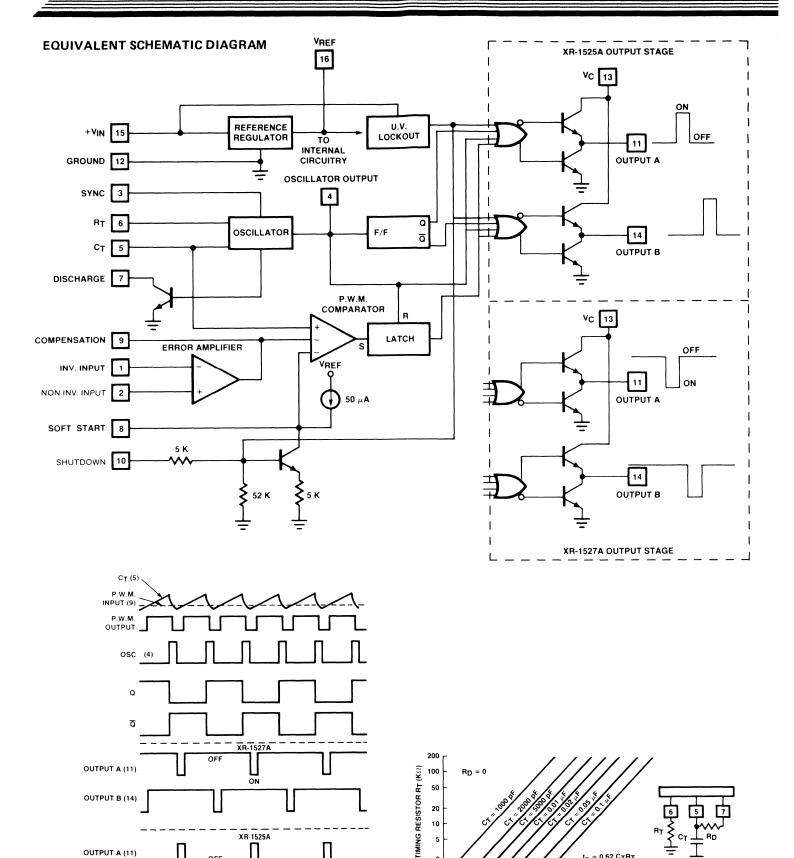


Figure 1: Typical Waveforms - XR-1525A/1527A.

XR-1525A

OUTPUT B (14)

OUTPUT A (11)

OUTPUT B (14)

Figure 2: Oscillator Charge Time vs. R<sub>T</sub> and C<sub>T</sub>.

50 100 200

CHARGE TIME ( $\mu$ sec)

10

= 0.62 CTRT

500 1 ms 2 ms 5 ms 10 ms

50

20 10



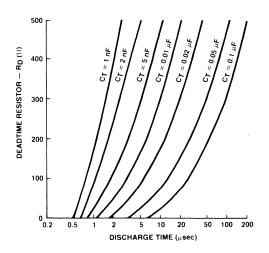


Figure 3: Oscillator Discharge Time vs  $R_D$  and  $C_T$ .

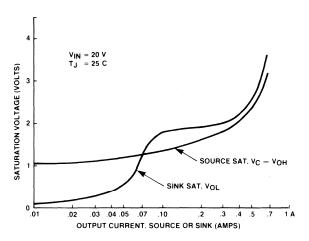


Figure 5: Output Saturation Characteristics.

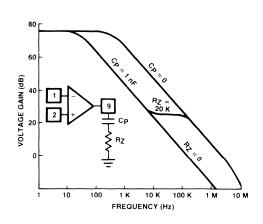


Figure 4: Error Amplifier Open-Loop Frequency Response.

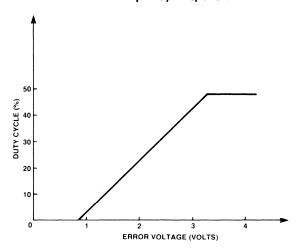


Figure 6: Output Duty Cycle vs. Error Voltage.

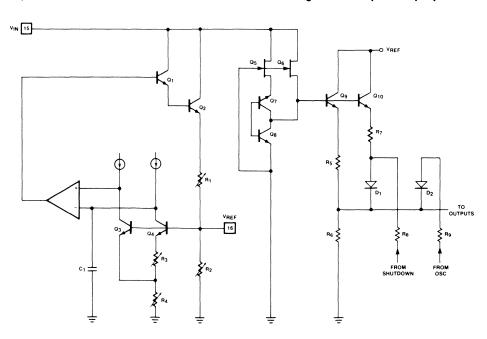


Figure 7: Equivalent Schematic of Voltage Reference Section.



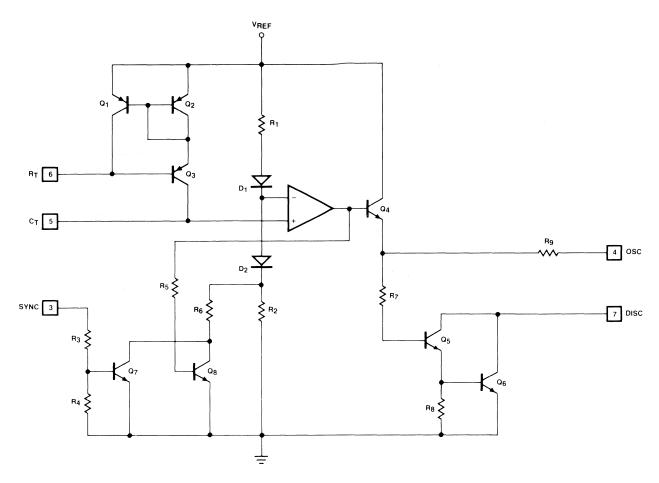


Figure 8: Equivalent Schematic of the Oscillator Section.

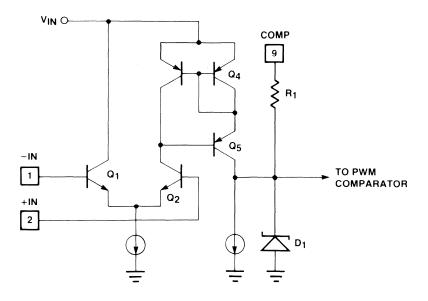


Figure 9: Equivalent Schematic of Error Amplifier Section.



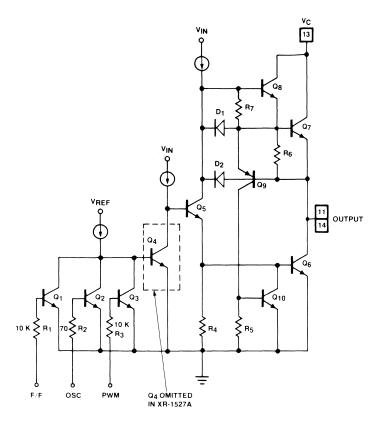


Figure 10: Equivalent Schematic of Output Drivers.

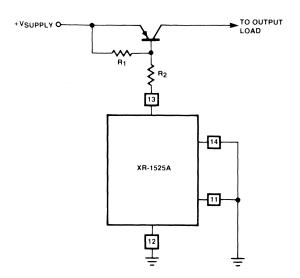


Figure 11: Single-Ended Output for XR-1525A.

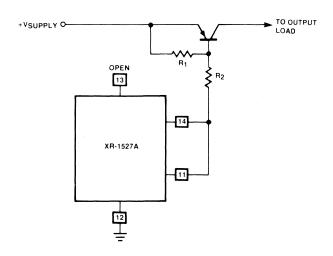


Figure 12: Single-Ended Output for XR-1527A.

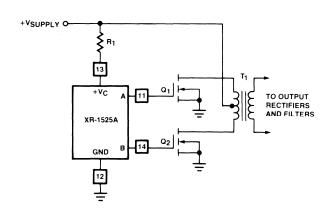


Figure 13: Push-Pull Outputs with XR-1525A.



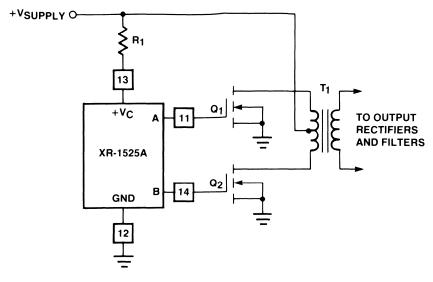


Figure 14: Power FET Push-Pull Outputs with XR-1525A.

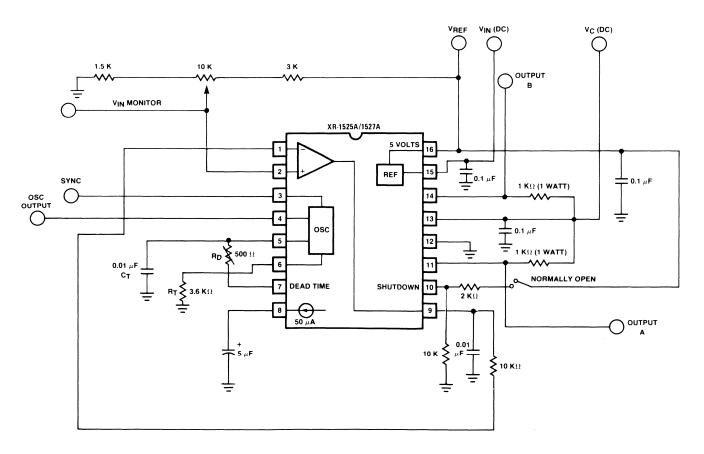


Figure 15: Generalized Test Circuit.



# **Power Supply Output Supervisory Circuit**

# **GENERAL DESCRIPTION**

The XR-1543/2543/3543 are monolithic integrated circuits that contain all the functions necessary to monitor and control the output of a power supply system. Included in the 16-Pin dual-in-line package is a voltage reference, an operational amplifier, voltage comparators, and a high-current SCR trigger circuit. The functions performed by this device include over-voltage sensing, under-voltage sensing and current limiting, with provisions for triggering an external SCR "crowbar."

The internal voltage reference on the XR-1543 is guaranteed for an accuracy of  $\pm$  1% to eliminate the need for external potentiometers. The entire circuit may be powered from either the output that is being monitored or from a separate bias voltage.

# **FEATURES**

Over-Voltage Sensing Capability
Under-Voltage Sensing Capability
Current Limiting Capability
Reference Voltage Trimmed ± 1%
SCR "Crowbar" Drive 300 mA
Programmable Time Delays
Open Collector Outputs
and Remote Activation Capability
Total Standby Current Less than 10 mA

# **APPLICATIONS**

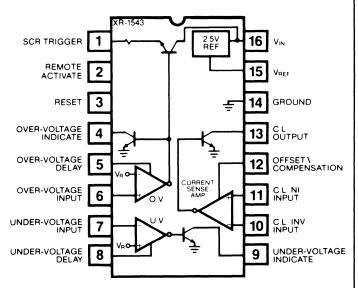
DC/DC Converters Power Line Monitors
Switch Mode Power Supplies Linear Power Supplies

#### **ABSOLUTE MAXIMUM RATINGS**

Input Supply Voltage, V <sub>IN</sub>	40V
Sense Inputs	$V_{IN}$
SCR Trigger Current (Note 1)	300 mA
Indicator Output Voltage	40V
Indicator Output Sink Current	50 mA
Power Dissipation (Ceramic)	1000 mW
Derate Above T <sub>A</sub> = +25°C	8.0 mW/°C
Power Dissipation (Plastic)	625 mW
Derate Above T <sub>A</sub> = 25°C	5.0 mW/°C
Operating Junction Temperature (T <sub>J</sub> )	+150°C
Storage Temperature Range	-65°C to +150°C

Note 1: At higher input voltages, a dissipation limiting resistor, R<sub>G</sub>, is required.

# **FUNCTIONAL BLOCK DIAGRAM**



# **ORDERING INFORMATION**

Part Number	Package	Operating Temperature
XR-1543M	Ceramic	-55°C to +125°C
XR-2543N	Ceramic	-25°C to +85°C
XR-3543N	Ceramic	0°C to +70°C
XR-3543P	Plastic	0°C to +70°C

# SYSTEM DESCRIPTION

An output supervisory circuit, such as the XR-1543, is used to control and monitor the performance of a power supply. In many systems, it is crucial that the supply voltage is always within some minimum and maximum level, to guarantee proper performance, and to prevent damage to the system. If the supply voltage is out of tolerance, it is often desirable to shut down the system or to have some form of indication to the operator or system controller. As well as protecting the system, the power supply sometimes needs to be protected under short circuit and current overload situations. By providing an SCR "crowbar" on the output of a power supply, it can be shut off under certain fault conditions as well.

The over-voltage sensing circuit (O.V.) can be used to monitor the output of a power supply and provide triggering of an SCR, when the output goes above the prescribed voltage level. The under-voltage sensing circuit (U.V.) can be used to monitor either the output of a power supply or the input line voltage.



# **ELECTRICAL CHARACTERISTICS**

**Test Conditions:**  $V_{IN} = 10V$ ,  $T_{J} = full operating temperature range, unless otherwise specified. Refer to Figure 9 for component designation.$ 

040445750	X	R-1 <b>543</b> /2	543		XR-3543		113117	CONDITIONS	
PARAMETER	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	CONDITIONS	
Input Voltage Range	4.5		40	4.5		40	<b>V</b>	T <sub>J</sub> = 25°C to max	
Input Voltage Range	4.7		40	4.7		40	V	T <sub>I</sub> = min to max	
Supply Current		7	10		7	10	mA	T <sub>J</sub> = 25°C, V <sub>IN</sub> = 40V	
REFERENCE VOLTAGE SECTIO	N (Pins 15 a	and 16)							
Output Voltage	2.48	2.50	2.52	2.45	2.50	2.55	V	T <sub>J</sub> = 25°C	
Output Voltage	2.45		2.55	2.40		2.60	V	T <sub>J</sub> = min to max	
Line Regulation		1	5		1	5	mV	V <sub>IN</sub> = 5 to 30V	
Load Regulation	12	1 15	10 25	12	1 15	10 25	mV mA	I <sub>ref</sub> = 0 to 10 mA	
Short Circuit Current Temperature Stability	'2	50	25	12	50	25	ppm/°C	V <sub>ref</sub> = 0V	
SCR TRIGGER SECTION (Pins 1, 2, and 3)									
Peak Output Current	100	200	400	100	200	400	mA	$V_{IN} = 5V, R_G = 0\Omega, V_O = 0$	
Peak Output Voltage	12	13	""	12	13	100	V	V <sub>IN</sub> = 15V, I <sub>O</sub> = 100 mA	
Output OFF Voltage	'-	0	0.1	'-	0	0.1	v	$V_{IN} = 40V$	
Remote Activate Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND	
Remote Activate Voltage	1	2	6		2	6	V	Pin 2 = Open	
Reset Current		0.4	0.8		0.4	0.8	mA	Pin 2 = GND, Pin 3 = GND	
Reset Voltage		2	6		2	6	V	Pin 2 = GND, Pin 3 = Open	
Output Current Slew Rate		400	1		400		mA/μs	$T_J = 25^{\circ} C, R_L = 50\Omega, C_D = 0$	
Propagation Delay Time		300	1		300		nsec	Tj = 25°C, R  = 50Ω,	
(From Pin 2)			1					C <sub>D</sub> = 0, Pin 2 = 0.4V	
Propagation Delay Time		500	1		500	1	nsec	$T_{J} = 25^{\circ} C, R_{I} = 50 \Omega,$	
(From Pin 6)								C <sub>D</sub> = 0, Pin 6 = 2.7V	
COMPARATOR SECTIONS (Pins 4	1, 5, 6, 7, 8	, and 9)	-						
Input Threshold	2.45	2.50	2.55	2.40	2.50	2.60	V	T <sub>J</sub> = 25°C	
(Input Voltage Rising on			1 1						
Pin 6 & Falling on Pin 7)	2.40		2.60	2.35		2.65	l v	T <sub>J</sub> = min to max	
Input Hysteresis		25	1 1				1		
		23	1 1	1	25		mV	-	
Input Bias Current		0.3	1.0		0.3	1.0	m∨ µA	Sense input = 0V	
Delay Saturation		0.3 0.2	0.5		0.3 0.2	0.5	μA V	Sense input = 0V	
Delay Saturation Delay High Level		0.3 0.2 6	0.5 7		0.3 0.2 6	0.5 7	μΑ ∨ ∨	·	
Delay Saturation Delay High Level Delay Charging Current	200	0.3 0.2 6 250	0.5 7 300	200	0.3 0.2 6 250	0.5 7 300	μΑ ∨ ∨ μΑ	V <sub>D</sub> = 0V	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage	200	0.3 0.2 6 250 0.2	0.5 7 300 0.5	200	0.3 0.2 6 250 0.2	0.5 7 300 0.5	μΑ ∨ ∨ μΑ ∨	V <sub>D</sub> = 0V I <sub>L</sub> = 10 mA	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current	200	0.3 0.2 6 250 0.2 0.01	0.5 7 300	200	0.3 0.2 6 250 0.2 0.01	0.5 7 300	µА V V µА V µА	V <sub>D</sub> = 0V I <sub>L</sub> = 10 mA V <sub>out</sub> = 40V	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage	200	0.3 0.2 6 250 0.2	0.5 7 300 0.5	200	0.3 0.2 6 250 0.2	0.5 7 300 0.5	μΑ ∨ ∨ μΑ ∨	V <sub>D</sub> = 0V I <sub>L</sub> = 10 mA V <sub>out</sub> = 40V C <sub>D</sub> = 0 } Pin 6 = 2.7V	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current	200	0.3 0.2 6 250 0.2 0.01	0.5 7 300 0.5	200	0.3 0.2 6 250 0.2 0.01	0.5 7 300 0.5	µА V V µА V µА	V <sub>D</sub> = 0V I <sub>L</sub> = 10 mA V <sub>out</sub> = 40V	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time		0.3 0.2 6 250 0.2 0.01 400	0.5 7 300 0.5 1.0	200	0.3 0.2 6 250 0.2 0.01 400	0.5 7 300 0.5	μΑ V V μΑ V μΑ nsec	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{\text{out}} = 40V$ $C_D = 0$ Pin 6 = 2.7V Pin 7 = 2.3V	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time CURRENT LIMIT AMPLIFIER SE		0.3 0.2 6 250 0.2 0.01 400 10	0.5 7 300 0.5 1.0	200	0.3 0.2 6 250 0.2 0.01 400	0.5 7 300 0.5	μΑ V V μΑ V μΑ nsec	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{out} = 40V$ $C_D = 0$ Pin 6 = 2.7V  Pin 7 = 2.3V $C_D = 1 \mu \text{F}$ $T_J = 25^{\circ} \text{C}$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current	CTION (Pi	0.3 0.2 6 250 0.2 0.01 400 10 ns 10, 11, 1	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0		0.3 0.2 6 250 0.2 0.01 400 10	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0	μΑ V μΑ V μΑ nsec msec	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{out} = 40V$ $C_D = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_D = 1 \mu F$ $T_J = 25^{\circ}C$ Pin 12 = Open, $V_{CM} = 0V$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage	CTION (Pid	0.3 0.2 6 250 0.2 0.01 400 10 ns 10, 11, 1	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10	0	0.3 0.2 6 250 0.2 0.01 400 10	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15	μΑ V μΑ V μΑ nsec msec	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{out} = 40V$ $C_D = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_D = 1 \mu F$ $T_J = 25^{\circ}C$ Pin 12 = Open, $V_{CM} = 0V$ $T_{CM} = 0V$ $T_{CM} = 0V$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage	CTION (Pi	0.3 0.2 6 250 0.2 0.01 400 10 ns 10, 11, 1	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0		0.3 0.2 6 250 0.2 0.01 400 10	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0	μΑ V μΑ V μΑ nsec msec	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{out} = 40V$ $C_D = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_D = 1 \mu F T_J = 25^{\circ} C$ Pin 12 = Open, $V_{CM} = 0V$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode	CTION (Pin	0.3 0.2 6 250 0.2 0.01 400 10 10 0.3 0 100	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10	0 70	0.3 0.2 6 250 0.2 0.01 400 10	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15	μΑ V μΑ V μΑ nsec msec	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} \text{T}_{J} = 25^{\circ} \text{C}$ $Pin 12 = \text{Open}, V_{CM} = 0V$ $Pin 12 = 0 \text{ pen}, V_{CM} = 0V$ $Pin 12 = 10 \text{ k}\Omega \text{ to GND}$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio	0 80 60	0.3 0.2 6 250 0.2 0.01 400 10 10 0.3 0 100 70	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10	70 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15	μΑ V μΑ ν μΑ nsec msec V μΑ mV mV	$V_D = 0V$ $I_L = 10 \text{ mA}$ $V_{\text{out}} = 40V$ $C_D = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_D = 1 \mu \text{F} / T_J = 25^{\circ}\text{C}$ Pin 12 = Open, $V_{\text{CM}} = 0V$ $Pin 12 = Open, V_{\text{CM}} = 0V$ $Pin 12 = 10 \text{ k}\Omega \text{ to GND}$ $V_{\text{IN}} = 15V, 0 \leq V_{\text{CM}} \leq 12V$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio Open Loop Gain	CTION (Pin	0.3 0.2 6 250 0.2 0.01 400 10 10 0.3 0 100 70 80	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10 120	0 70	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15 130	μΑ V μΑ ν μΑ nsec msec V μΑ mV mV dB dB	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} \text{T}_{J} = 25^{\circ} \text{C}$ $Pin 12 = \text{Open}, V_{CM} = 0V$ $Pin 12 = 0 \text{pen}, V_{CM} = 0V$ $Pin 12 = 10 \text{ k}\Omega \text{ to GND}$ $V_{IN} = 15V, 0 \leq V_{CM} \leq 12V$ $V_{CM} = 0V, \text{Pin } 12 = \text{Open}$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio Open Loop Gain Output Saturation Voltage	0 80 60	0.3 0.2 6 250 0.2 0.01 400 10 10 0.3 0 100 70 80 0.2	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10 120	70 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15 130	μΑ V μΑ ν μΑ nsec msec V μΑ mV dB dB V	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} \text{T}_{J} = 25^{\circ} \text{C}$ $Pin 12 = \text{Open}, V_{CM} = 0V$ $Pin 12 = \text{Open}, V_{CM} = 0V$ $Pin 12 = 10 \text{ k}\Omega \text{ to GND}$ $V_{IN} = 15V, 0 \leq V_{CM} \leq 12V$ $V_{CM} = 0V, \text{Pin } 12 = \text{Open}$ $I_{L} = 10 \text{ mA}$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio Open Loop Gain Output Saturation Voltage Output Leakage Current	0 80 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10 120	70 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15 130	μΑ V μΑ ν μΑ nsec msec V μΑ mV mV dB dB V μΑ	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} \int T_{J} = 25^{\circ} \text{C}$ Pin 12 = Open, $V_{CM} = 0V$ $Pin 12 = Open, V_{CM} = 0V$ $Pin 12 = 10 \text{ k} \Omega \text{ to GND}$ $V_{IN} = 15V, 0 \leq V_{CM} \leq 12V$ $V_{CM} = 0V, Pin 12 = Open$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio Open Loop Gain Output Saturation Voltage Output Leakage Current Small Signal Bandwidth	0 80 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01 5	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10 120	70 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01 5	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15 130	μΑ V μΑ ν μΑ nsec msec V μΑ mV mV dB dB V μΑ MHz	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} T_{J} = 25^{\circ} \text{C}$ Pin 12 = Open, $V_{CM} = 0V$ $Pin 12 = Open, V_{CM} = 0V$ $Pin 12 = 10 \text{ k} \Omega \text{ to GND}$ $V_{IN} = 15V, 0 \leq V_{CM} \leq 12V$ $V_{CM} = 0V, Pin 12 = Open$ $I_{L} = 10 \text{ mA}$ $V_{out} = 40V$ $T_{J} = 25^{\circ} \text{C}, Av = 0 \text{ dB}$	
Delay Saturation Delay High Level Delay Charging Current Indicate Saturation Voltage Indiate Leakage Current Propagation Delay Time Propagation Delay Time  CURRENT LIMIT AMPLIFIER SE Input Voltage Range Input Bias Current Input Offset Voltage Input Offset Voltage Common Mode Rejection Ratio Open Loop Gain Output Saturation Voltage Output Leakage Current	0 80 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01	0.5 7 300 0.5 1.0 2, and 13) V <sub>IN</sub> -3V 1.0 10 120	70 60	0.3 0.2 6 250 0.2 0.01 400 10 0.3 0 100 70 80 0.2 0.01	0.5 7 300 0.5 1.0 V <sub>IN</sub> -3V 1.0 15 130	μΑ V μΑ ν μΑ nsec msec V μΑ mV mV dB dB V μΑ	$V_{D} = 0V$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$ $C_{D} = 0$ $Pin 6 = 2.7V$ $Pin 7 = 2.3V$ $C_{D} = 1 \mu \text{F} T_{J} = 25^{\circ} \text{C}$ Pin 12 = Open, $V_{CM} = 0V$ $Pin 12 = Open, V_{CM} = 0V$ $Pin 12 = 10 \text{ k} \Omega \text{ to GND}$ $V_{IN} = 15V, 0 \leq V_{CM} \leq 12V$ $V_{CM} = 0V, Pin 12 = Open$ $I_{L} = 10 \text{ mA}$ $V_{Out} = 40V$	



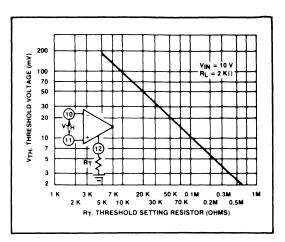


Figure 1: Current Limiting Threshold (V<sub>TH</sub>) vs. Threshold Setting Resistor (R<sub>T</sub>).

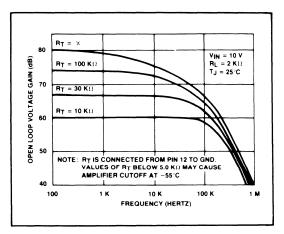


Figure 3: Current Limiting Amplifier Gain vs. Threshold Setting Resistor  $(R_T)$ .

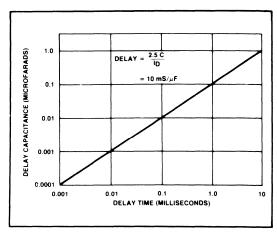


Figure 5: Comparator Activation Delay vs. Capacitor Value.

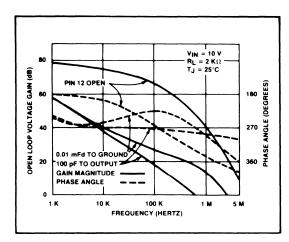


Figure 2: Current Limiting Amplifier – Frequency Response.

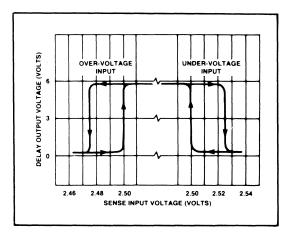


Figure 4: Over-Voltage and Under-Voltage Comparator Hysteresis.

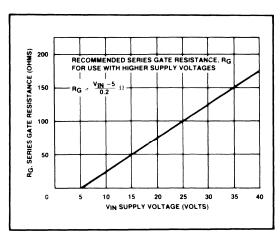


Figure 6: SCR Trigger -- Series Gate Resistance (R<sub>G</sub>) vs. Input Voltage.





# PRINCIPLES OF OPERATION

The internal control blocks of the XR-1543 operate as follows:

### **Voltage Reference Section**

The internal voltage reference circuit of the XR-1543 is based on the well-known "band-gap reference" with a nominal output voltage of 2.50 volts, internally trimmed to give an accuracy of  $\pm$  1% at 25°C. It is capable of providing a stable output voltage over a wide input voltage range. Furthermore, its performance is guaranteed for changes in line and load conditions. The accuracy of the output voltage is guaranteed to  $\pm$  2% maximum for the XR-1543/2543, and  $\pm$  4% maximum for the XR-3543, over the entire operating temperature range.

The output of the reference circuit is capable of providing up to 10 mA of current for use as a reference for external circuitry. The primary function of this circuit is to provide a very accurate and stable reference input for the undervoltage and over-voltage comparators, thereby enabling very precise monitoring of line and output voltages without potentiometers.

# **Comparator Section**

The under-voltage and over-voltage sensing comparators of the XR-1543 are identical except for the input polarities. Each section is made up of two comparators in series whose inputs are referenced to 2.50 volts. The delay terminal between the comparators requires an external capacitor to ground for programmable time delays on the output.

When an out-of-tolerance situation occurs, the first comparator activates a current source which then charges the external capacitor at a constant rate. This ramp voltage is then compared to the reference voltage by the second comparator which activates the output indicating circuit. With no external capacitor, the overall time delay from sense input to output is approximately 0.5  $\mu$ sec. The charging current for the capacitor,  $C_D$ , is approximately 250  $\mu$ A which results in the following relationship:

Time delay =  $10 C_D$  (msec)

where  $C_D$  is in  $\mu F$ .

The output npn transistors are capable of sinking 10 mA with saturation voltage of less than 0.4 volts. The outputs can be "wired OR'd" to provide a single output indicator.

#### **Current Sensing Amplifier**

The operational amplifier used in the XR-1543 is a high-gain, externally compensated amplifier with open collector

outputs. The pnp input stage provides for a wide input common mode range extending from ground to approximately 3 volts below the positive supply. With a  $2\,\mathrm{k}\Omega$  pullup resistor, the open-loop voltage gain is 72 dB minimum with a unity gain bandwidth beyond 5 MHz. The operational amplifier may be used as a comparator or, if linear amplification is required, external compensation may be added for stable performance over a wide frequency range.

The input offset voltage of this amplifier is specified for 10 mV maximum; however, it may be programmed externally for thresholds up to 200 mV. By connecting a resistor, R  $_{T}$ , from Pin 12 to ground, the input threshold voltage can be varied. For most current sensing applications, the required threshold polarity calls for a positive voltage on the inverting input. Reducing the impedance on Pin 12 also lowers the overall voltage gain of the amplifier, which makes this pin a convenient point to apply frequency compensation. This can be accomplished by either connecting  $\rm C_1$  to the output, or  $\rm C_2$  to ground as shown in Figure 8. The diode,  $\rm D_1$ , and the resistor,  $\rm R_C$ , are used only if it is necessary to increase the frequency response by operating the output at a higher current and/or isolating the load from  $\rm R_C$  and  $\rm C_1$ , when the amplifier is off.

#### **SCR Trigger Section**

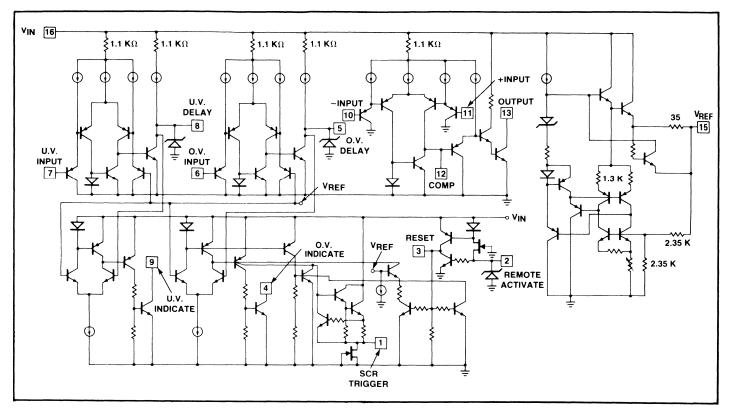
The SCR trigger section of the XR-1543 is connected to the output of the over-voltage comparator and is capable of handling 300 mA. The circuit also provides for remote activation of the output as well as a reset terminal. When an over-voltage situation occurs, the output of the sensing comparator goes low, turning "on" the over-voltage indicate transistor. At the same time, the comparator drives an npn Darlington pair which provides 300 mA to activate an external SCR crowbar.

A remote activation circuit is included to allow the user to activate the SCR crowbar in other than an over-voltage situation. When this terminal, Pin 2, is grounded, it forces the output of the comparator low which activates the output circuitry in the same manner as the over-voltage comparator does.

Another function of this circuit is to provide the capability to latch the O.V. indicate and SCR trigger outputs "on", after a fault is sensed. This is done by connecting the remote activate terminal (Pin 2) to the O.V. indicating terminal (Pin 4). When an O.V. condition occurs, Pin 2 is pulled low, which in turn holds the outputs in the "on" condition until the reset terminal is externally grounded, removing the latch and turning "off" the outputs. If the external connection is not made, the high current output will be activated only as long as a fault condition exists. When the fault condition disappears, the outputs will be disabled. The thresholds for both remote activation and reset terminals are approximately 1.2 volts.



# **EQUIVALENT SCHEMATIC DIAGRAM**



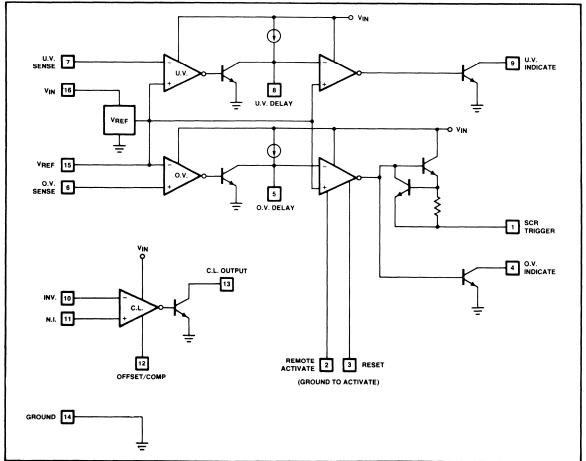


Figure 7: XR-1543 Block Diagram.



# **APPLICATIONS INFORMATION**

A typical application of the XR-1543 is to monitor a single power supply output voltage as shown in Figure 9. In this circuit, both over- and under-voltage sensing and current-limiting functions are performed. The circuit shown is powered from an external bias capable of supplying 10 mA in addition to the activation current for the SCR trigger. With Pin 2 tied to Pin 4, a latch has been provided such that when an over-voltage situation occurs, the o.v. indicator and SCR trigger are activated and held until the reset terminal is externally grounded.

In powering an SCR from supply voltages greater than 5 volts, an external resistor,  $R_{G}$ , is required on Pin 1 to limit the power dissipation for the XR-1543. Although the XR-1543 is capable of handling 300 mA of current, its power dissipation must be kept below the absolute maximum ratings.

In this circuit, current-limiting is performed by sensing the voltage drop across the resistor,  $R_{SC}$ , in the positive supply line. The threshold for the amplifier is externally set by the resistor,  $R_{T}$ .

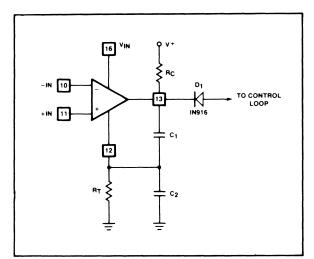


Figure 8: Current Limiting Amplifier Connections for Threshold Control and Frequency Compensation.

The values of the external components used in Figure 9 are calculated as follows:

- 1. Current limiting threshold,  $V_{TH} \approx \frac{1000}{R_T}$
- 2. C<sub>1</sub> is determined by the loop dynamics.
- 3. Peak current to load,

$$I_P \approx \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}} \left(\frac{R_2}{R_2 + R_3}\right)$$

4. Short circuit current.

$$I_{SC} = \frac{V_{TH}}{R_{SC}}$$

5. Low output voltage limit,

$$V_O (low) = \frac{2.5(R_4 + R_5 + R_6)}{R_5 + R_6}$$

6. High output voltage limit,

$$V_O \text{ (high)} = \frac{2.5(R_4 + R_5 + R_6)}{R_6}$$

- 7. Voltage sensing delay,  $T_D = 10,000 C_D$
- 8. SCR trigger power limiting resistor,

$$R_{G} > \frac{V_{IN} - 5}{0.2}$$



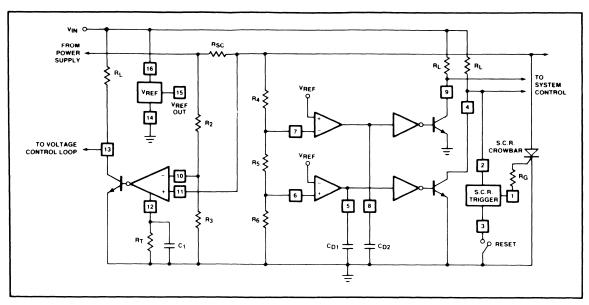


Figure 9: Typical Connection for Linear Foldback Current Limiting as well as Over-Voltage and Under-Voltage Protection.

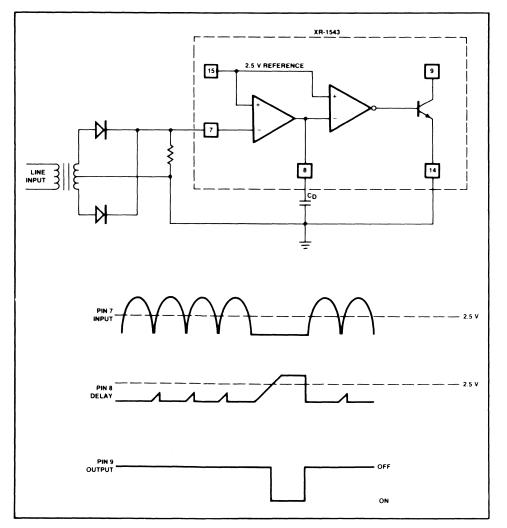


Figure 10: XR-1543 - Input Line Monitor Circuit.



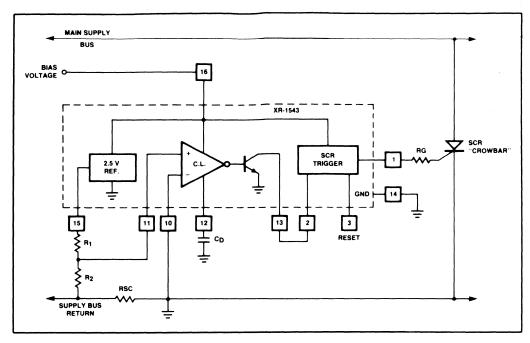


Figure 11: XR-1543 - Over Current Shutdown Circuitry.

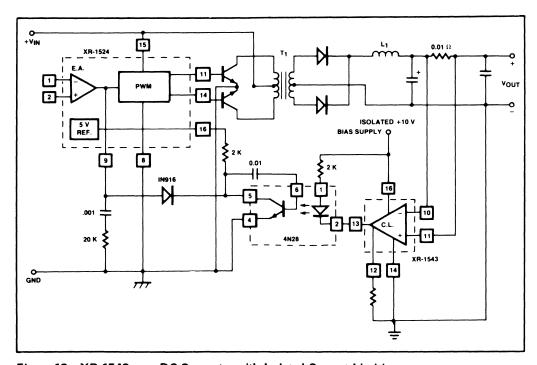


Figure 12: XR-1543 - DC Converter with Isolated Current Limiting.



# Pulse-Width Modulator Control System

# **GENERAL DESCRIPTION**

The XR-2230 is a high-performance monolithic pulsewidth modulator control system. It contains all the necessary control blocks for designing switch mode power supplies, and other power control systems. Included in the 18-Pin dual-in-line package are two error amplifiers, a sawtooth generator, and the necessary control logic to drive two open-collector power transistors. Also included are protective features, such as adjustable dead-time control, thermal shutdown, soft-start control, and doublepulse protection circuitry.

The device provides two open-collector output transistors which are driven 180° out-of-phase, and are capable of sinking 30 mA. These outputs can be used to implement single-ended or push-pull switching regulation of either polarity in transformerless or transformer-coupled converters.

# **FEATURES**

Thermal Shutdown Adjustable Dead-time Dual Open-Collector 30 mA Output Transistors Double-Pulse Protection Circuit Soft-Start Control High-Speed Remote Shut-Down Input Two High-Performance Error Amplifiers with ± 5V Input Common-Mode Range

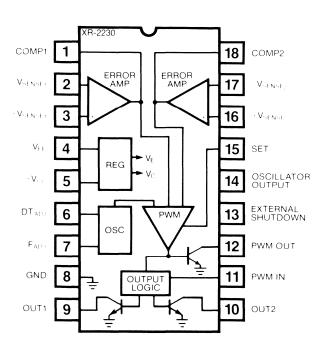
# **APPLICATIONS**

Switching Regulators Motor-Speed Controllers Pulse-Width Modulated Control Systems

#### **ABSOLUTE MAXIMUM RATINGS**

Positive Supply Voltage	-0.5 to +18V
Negative Supply Voltage	+0.5 to -18V
Input Voltage	-18 to +18V
Output Voltage	-0.5 to $+18$ V
Power Dissipation ( $T_A \le 25^{\circ}$ C)	400 mW
Operating Temperature	-10°C to +85°C
Storage Temperature	-55°C to +125°C

# **FUNCTIONAL BLOCK DIAGRAM**



# ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2230CP	Plastic	0°C to +70°C

### SYSTEM DESCRIPTION

The XR-2230 PWM circuit contains two high-performance error amplifiers with wide input common-mode range, and large voltage gains. Typically, one amplifier (Pins 16, 17, 18) is used for current sensing and the other (Pins 1, 2, 3) is used as an error amplifier to sense the output voltage. The XR-2230 requires a split supply between ± 8 volts and ± 15 volts, however, it can be operated from a single supply with proper external biasing on the ground pin and input pins of the error amplfiers. The output drivers capable of sinking 30 mA at a saturation voltage of about 0.3V can be used in a push-pull configuration, or can be paralled for a single-ended configuration with a duty cycle between 0% to over 90%.

The XR-2230 features a self-protecting thermal-shutdown circuitry which turns off the output drivers when the junction temperature exceeds 130°C. The on-board regulator stabilizes the oscillator frequency to 0.1%/V for reliable performance.



# **ELECTRICAL CHARACTERISTICS**

**Test Conditions:**  $T_A = 25^{\circ}C$ ,  $V_{CC} = +12V$ ,  $V_{EE} = -12V$ ,  $f_{OSC} = 20$  kHz, unless otherwise specified.

SYMBOL	PARAMETERS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
SUPPLY SE	ECTION	<u> </u>	L	L	1	
VCC VEE ICC IEE	Positive Supply Voltage Negative Supply Voltage Positive Supply Current Negative Supply Current	+10 7.0 -2.0	11.0 -6.0	-10 15.0 -2.0	V V mA mA	
OSCILLAT	OR SECTION	<u> </u>	<u> </u>		L	
rosc Vosc δ	Frequency Range Initial Accuracy Supply Voltage Stability Low Supply Voltage Temperature Stability Sawtooth Peak Voltage Duty Cycle Range	-20 3.0 10	0.1 0.01 3.5	100 15 +20 4.0 90	kHz % %/V % %/°C V %	R <sub>T</sub> = 30 kΩ, C <sub>T</sub> = 4700 pF V <sub>CC</sub> = +10V $\approx$ +15V V <sub>CC</sub> = +18V, V <sub>EE</sub> = -8V fosc = 20 kHz
VOLTAGE	ERROR AMPLIFIER			•	I	
VOS IBIAS AVO f_3dB CMRR	Input Offset Voltage Input Bias Current Open-Loop Gain Closed-Loop Bandwidth Common-Mode	60	2 5 90 25	10 -30	mV μA dB kHz	AVCL = 40 dB
Voм	Rejection Ratio Output Voltage Swing	60 ± 5			dB V	$V_{ICM} = \pm 4.5V$ $R_L = 10 \text{ k}\Omega$
SR	Slew Rate Input Voltage Range	2	4 ± 5		V/ <b>μ</b> s V	$V_{CC} = +8V$ , $V_{EE} = -8V$ $A_{VCL} = 14 \text{ dB}$ , $R_F = 10 \text{ k}\Omega$
CURRENT	ERROR AMPLIFIER				4	*
VOS IBIAS AVO f-3dB CMRR	Input Offset Voltage Input Bias Current Open-Loop Gain Closed-Loop Bandwidth Common-Mode	60	4 -1.0 90 25	20 -60	mV μΑ dB kHz	AVCL = 40 dB
Voм	Rejection Ratio Output Voltage Swing	60 ± 5 ± 4	90		dB V V	$V_{ICM} = \pm 4.5V$ $R_{L} = 10 \text{ k}\Omega$ $V_{CC} = +8V, V_{EE} = -8V$
SR	Slew Rate Input Voltage Range	4	8 ± 5		∨/μs ∨	$AVCL = 14 dB, RF = 10 k\Omega$
MODULAT	OR SECTION					
t <sub>d</sub>	Set Input Open Voltage (Pin 15) Modin Input Open Voltage (Pin 11) Inhibit Input Current (Pin 13) Inhibit Propagation Delay Out1, Out 2, Output Voltage	3.1 2.8 3.1 2.8 -50	3.6 3.3 3.6 3.3 -10 60	4.1 4.3 4.1 4.3	∨ ∨ ∨ μ ns ∨	V <sub>CC</sub> = +8V, V <sub>EE</sub> = -8V V <sub>CC</sub> = +8V, V <sub>EE</sub> = -8V I <sub>O</sub> = 30 mA, T <sub>A</sub> = 25°C
tf	(Pins 9 & 10) Low Supply Voltage Out1, Out2 Fall Time Modout Output Voltage (Pin 12) Under Low Supply Voltage Oscillator Output Voltage (Pin 14)		30	0.4 0.3 0.4 0.3 0.4 0.6	V V ns V V V	$T_A = -10 \approx +85^{\circ} C$ $I_O = 27 \text{ mA}, T_A = 25^{\circ} C$ $I_O = 16 \text{ mA}, T_A = 25^{\circ} C$ $T_A = -10 \approx +85^{\circ} C$ $I_O = 14 \text{ mA}, T_A = 25^{\circ} C$ $I_O = 3 \text{ mA}, T_A = 25^{\circ} C$ $T_A = -10 \approx +85^{\circ} C$
	Thermal Shutdown Temp.		130		°C	



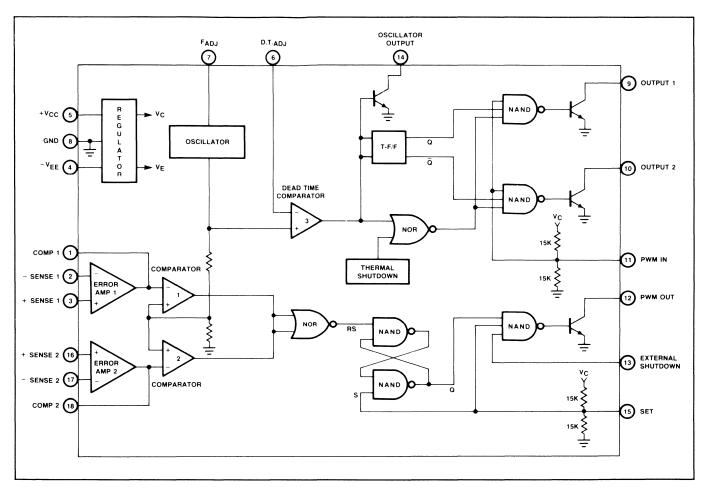


Figure 1. Equivalent Schematic Diagram

#### PRINCIPLES OF OPERATION

The heart of the XR-2230 is the sawtooth generator. As seen in Figure 1, this sawtooth drives one input of each of the three system comparators. Comparators one and two have their other inputs tied to the outputs of the error amplifiers. These comparators will now produce, at their outputs, square waves which will have a duty cycle proportional to the voltage at the inputs to the error amplifiers. or pulse width information. The pulse width information is fed into the NOR gate and used to provide the reset information to the pulse-width modulation flip-flop (PWM). The PWM flip-flop information is fed into the NAND gate with the external shutdown and PWM flip-flop set input. The information from the NAND gate drives an open-collector transistor to provide the pulse-width modulation output, Pin 12. The PWM output will be a square wave with a frequency set by the sawtooth generator, and a duty cycle equal to either comparator, one or two, whichever is shorter. If the external shutdown, Pin 13, is driven low, the PWM output will remain low or go to zero duty cycle. The set input of the PWM flip-flop, Pin 15, is normally connected to the buffered sawtooth generator output, Pin 14, so that a reset pulse is provided every cycle. Each output transistor is driven by a three input NAND gate. These inputs consist of:

- Pulse width information from the PWM input, Pin 11, which is used to control the off time of the output transistors. The PWM input is normally tied to the PWM output so that the output transistor's off time is a function of the error amplifier's input voltage.
- 2. Pulse-steering information from flip-flop two, which will determine which output transistor receives the PWM input signal. Flip-flop two will toggle once every cycle of the sawtooth generator's output, which will make the output transistor's toggle frequency one-half that of the sawtooth generator's.



3. Information from dead-time and thermal shutdown circuitry. The dead-time is an externally adjustable time between one output transistor turning off and the other turning on. This is used to protect external circuitry. This dead-time is controlled by an external voltage applied to Pin 6, which is internally compared with the sawtooth waveform. The thermal shutdown circuitry will drive the input to the NAND gate low, if the junction temperature exceeds 130°C. This will make both outputs low.

The circuit control blocks and functions operate as follows:

**Error Amplifiers** — These are high-gain op amps which are used to sense output conditions, voltage and current, and provide a dc voltage to comparators one and two. This will in turn adjust the PWM output duty cycle and ultimately that of the output transistors to correct for errors in the output voltage or overcurrent conditions. The amplifier's outputs are provided for tailoring the closed-loop gain or frequency response of the system. Figure 2 shows the relationship between output duty cycle, Pins 11 and 12 connected, and the voltage at Pins 1 or 18. Amplifier two is approximately twice as fast as Amplifier one, and should, therefore, be used to sense output current.

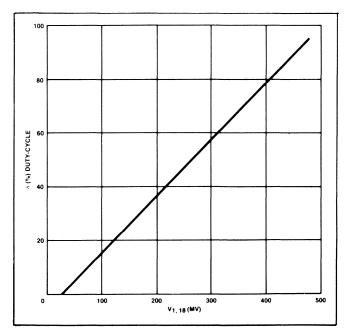


Figure 2. Modulation Duty Cycle vs Error Voltage

**External Shutdown, Pin 13** – A low level signal applied to this pin will turn both outputs on. If not used, this input should be left open-circuited. The impedance at this node is approximately 1  $M\Omega$ .

**Oscillator Output, Pin 14** — This is an open-collector output which will be a square wave with a frequency set by the sawtoogh generator. The duty cycle of this output will vary from 10 to 90%, and is a function of the dead-time setting. This pin is normally connected to Pin 15, set to provide reset pulses for the PWM flip-flop.

**Set, Pin 15** — This is the set input for the PWM flip-flop. A low-going signal at this pin will cause the flip-flop to be reset. The impedance at this pin is approximately 7.5 k $\Omega$ . This pin is normally connected to the oscillator output, Pin 14.

**PWM Out, Pin 12** — This is an open-collector output which provides a square wave with a duty cycle determined by the error amplifiers. This output is normally connected to PWM IN, Pin 11.

**PWM In, Pin 11** — This is the input which controls the duty cycle of the output transistors. A low level on this pin will drive both output transistors on. The impedance into this pin is approximately  $7.5~\mathrm{k}\Omega$ .

Output Transistors, Pins 9 and 10 — These pins provide the open-collector output transistors which are capable of sinking 30 mA, typically. They are alternately turned off,  $180^{\circ}$  out-of-phase, at a rate equal to one-half the frequency of the oscillator.

**FADJ. Pin 7** — A resistor,  $R_{ext}$  to + V<sub>CC</sub>, and a capacitor,  $C_{ext}$ , to ground from this pin, set the frequency of the sawtooth and oscillator output, by the relationship:

$$f_{OSC} = \frac{2.68}{R_{ext} \times C_{ext}}$$



The sawtooth waveform, a signal varying from zero volts to +5V, will be present at Pin 7. Normal values of  $R_{eXt}$  will range from 1 k $\Omega$  to 100 k $\Omega$ . Figure 3 shows the oscillator period as a function of various  $R_{eXt}$  and  $C_{ext}$  values.

The dead-time (minimum time from one output turning on to the other turning off) is controlled by the voltage applied to Pin 6.

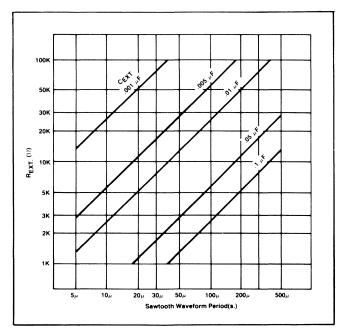


Figure 3. Oscillation Period vs REXT and CEXT

**Dead-time Control, Pin 6** — Figure 4 shows output dead-time as a function of VPIN 6. The maximum duty cycle of each output is also controlled by the dead-time, and may be determined by the following expression:

Duty Cycle Max (%) = 
$$(1 - \frac{.35}{VPIN 6}) \times 50\%$$
  
 $VPIN 6 < 3.5V$ 

The impedance into this pin is approximately 10 k $\Omega$ .

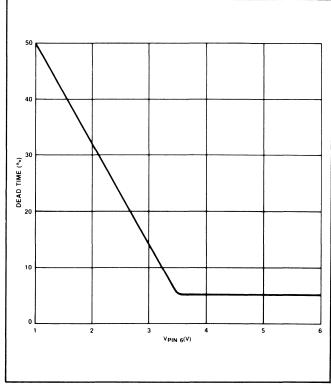


Figure 4. Dead Time vs Dead Time Adjustment Voltage

# RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION	UNIT
VCC	Positive Supply Voltage	+10 ≈ +15	V
VEE	Negative Supply Voltage	-10 ≈ -15	V
RR	Minimum Feedback Resistance	10	kΩ
Av	Minimum Voltage Gain	14 5	dB V/V



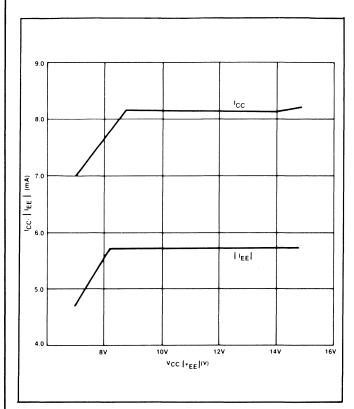


Figure 5. Supply Current vs Supply Voltage



The soft-start function may be implemented as shown in Figure 7. This configuration will reduce the output duty cycle to zero, and gradually increase to its normal operating point, whenever power is applied to the circuit, or after an external shutdown command has been given. This is used to keep the magnetics in the circuit from saturating.

The time for the duty cycle to start will be approximately equal to  $R_1 \times C_1$ .

A typical step-down switching regulator configuration is shown in Figure 8. Only one output transistor is used, so that the maximum duty cycle will be limited to 45%. If a larger duty cycle range is needed, the two outputs may be externally NOR'd as shown in Figure 9. This configuration will allow up to 90% duty cycles.

Figure 10 shows a detailed timing diagram of circuit operation.

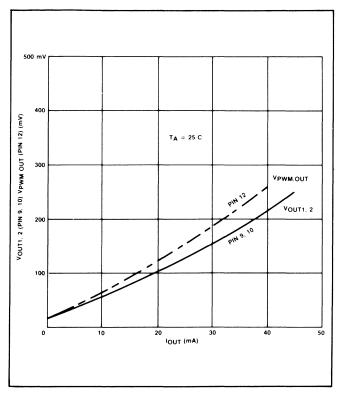


Figure 6. Output Saturation Voltage vs Load Current

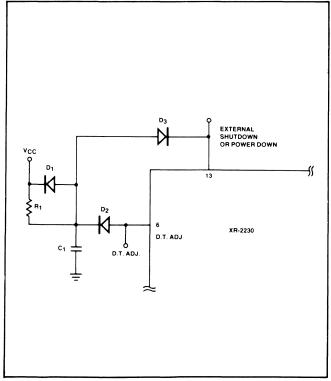


Figure 7. Soft Start Connection



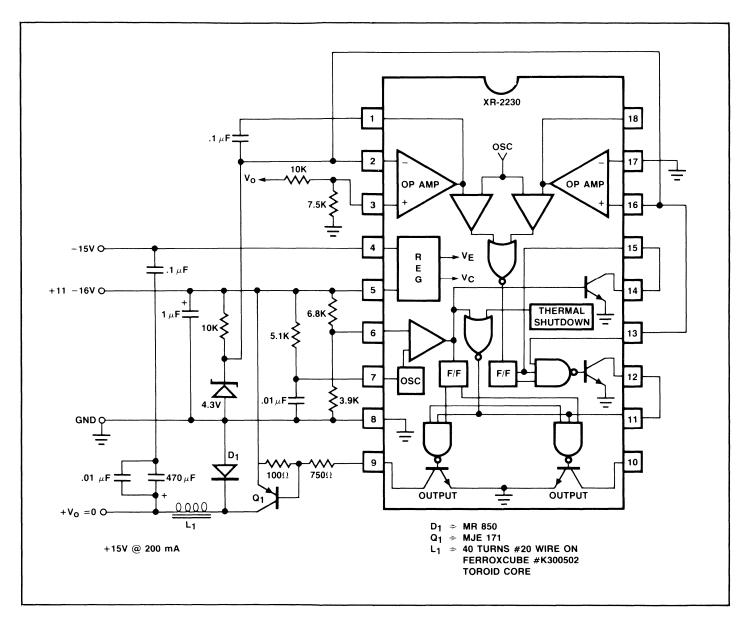


Figure 8: +10V Step-Down Regulator



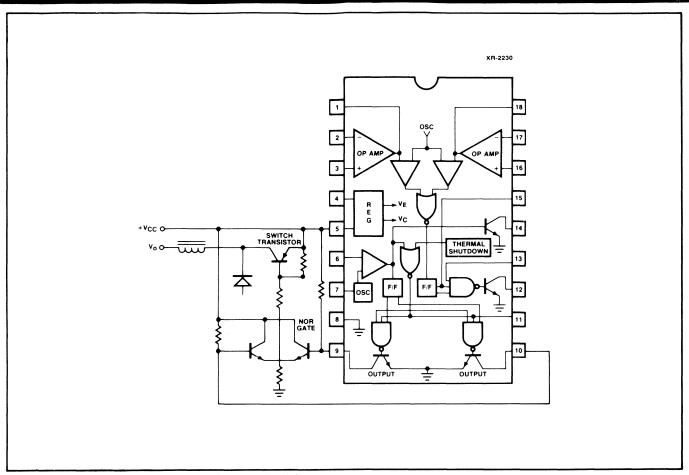


Figure 9. Outputs Nor'd for up to 90% Duty Cycle's

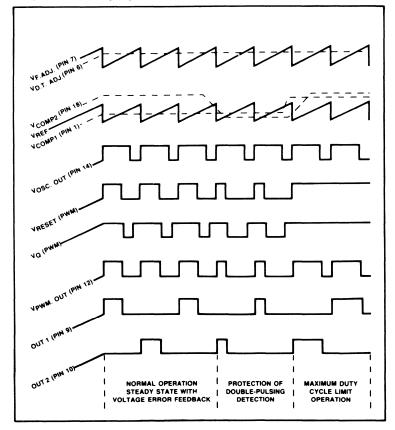


Figure 10. Timing Waveform Diagram

Vo-



# **Dual Tracking Voltage Regulators**

# **GENERAL DESCRIPTION**

The XR-4194 is a dual polarity tracing regulator designed to provide balanced or unbalanced posititive and negative output voltages at currents of up to 200 mA. A single resistor can be used to adjust both outputs between the limits of ±50 mV and ±42 V. The device is ideal for local on-card regulation, which eliminates the distribution problems associated with single-point regulation. The XR-4194 is available in a 14-pin ceramic dual-in-line package, which has a 900 mW rating.

#### **FEATURES**

Direct Replacement for RM/RC-4194 Both Outputs Adjust with Single Resistor Load Current to  $\pm$  200 mA with 0.2% Load Regulation Low External Parts Count Internal Thermal Shutdown at T<sub>J</sub> = 175°C External Adjustment for  $\pm$  V<sub>O</sub> Unbalancing

#### **APPLICATIONS**

On-Card Regulation in Analog and Digital Systems Main Regulation in Small Instruments Point-of-Load Precision Regulation

# **ABSOLUTE MAXIMUM RATINGS**

Input Voltage ±V to Ground XR-4194M ±45 V XR-4194CN ±35 V Input/Output Voltage Differential ±45 V Power Dissipation at  $T_A = 25^{\circ}C$ 900 mW Load Current 150 mA Operating Temperature Range -55°C to +150°C XR-4194M 0°C to +125°C XR-4194CN -65°C to +150°C Storage Temperature Range

# **FUNCTIONAL BLOCK DIAGRAM** +VIN POSITIVE REGULATOR 13 NC 12 COMP+ GND VOLTAGE RSET REFERENCE COMP 10 RO NEGATIVE 9 NC REGULATOR

# **ORDERING INFORMATION**

Part NumberPackageOperating TemperatureXR-4194MCeramic-55°C to +125°CXR-4194CNCeramic0°C to +70°C

# SYSTEM DESCRIPTION

The XR-4194 is a dual polarity tracking voltage regulator. An on board reference, set by a single resistor, determines both output voltages. Tracking accuracy is better than 1%. Non-symmetrical output voltages are obtained by connecting a resistor to the balance adjust (Pin 4). Internal protection circuits include thermal shutdown and active current limiting.



# **ELECTRICAL CHARACTERISTICS**

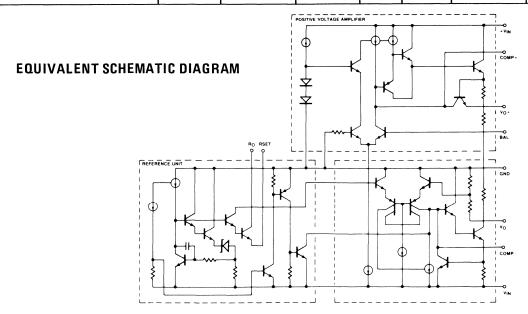
Test Conditions:  $\pm 5 \le V_{OUT} \le V_{MAX}$ : XR-4194M -55°C ≤ +125°C: XR-4194CN 0°C ≤ T<sub>J</sub> X +70°C

	Х	XR-4194M XR-4194CN						
PARAMETERS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Line Regulațion		0.02	0.1		0.02	0.1	%Vout	>V <sub>IN</sub> = 0.1 V <sub>IN</sub>
Load Regulation		0.001	0.0025		0.001	0.004	%VQ/mA	XR-4194CN, M:
							J .	I <sub>I</sub> = 5 to 100 mA
TC of Output Voltage		0.002	0.020		0.003	0.015	%/°C	_
*Stand-by Current Drain from		+0.3	+1.0		+0.3	+1.5		$V_{IN} = V_{MAX}, V_{O} = 0V$
							mΑ	
to		-1.2	-2.0		-1.2	-2.0		$V_{IN} = V_{MAX}, VO = 0V$
Input Voltage Range	±9.5		±45	±9.5		±35	V	
Output Voltage Scale Factor	2.45	2.5	2.55	2.38	2.5	2.62	KΩ/V	R <sub>SET</sub> = 71.5 K T <sub>J</sub> = 25°C
Output Voltage Range	0.05		+42	0.05		±35	V	R <sub>SET</sub> = 71.5 K
Output Voltage Tracking			1.0			2.0	%	
Ripple Rejection		70			70		dB	f - 120 Hz, TJ = 25°C
Input-Output Voltage Diff.	3.0			3.0			V	IL = 50 mA
Output Noise Voltage		250			250		μ∨ RMS	$C_{L} = 4.7 \mu\text{F},  \text{V}_{O} = \pm 15 \text{V}$
								f = 10 Hz to 100 kHz
Internal Thermal Shutdown		175			175		°C	
Internal Thermal	L			<u> </u>				- Comment of the Comm

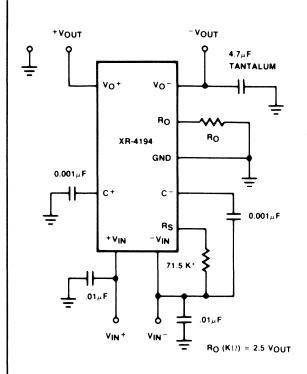
<sup>\*</sup> $\pm 1_{Quiescent}$  will increase by 50  $\mu$ A/V<sub>QUT</sub> on positive side and 100  $\mu$ A/V<sub>QUT</sub> on negative side.

# THERMAL CHARACTERISTICS

	XR-4194M			Х	R-4194C	N		
PARAMETERS	MIN	TYP	MAX	MIN	TYP	MAX	CONDITIONS	
Power Dissipation			900 mW 2.2 W			900 mW 2.2 W	T <sub>A</sub> = 25°C	
Thermal Resistance Junction to Ambient Junction to Case		128°C/W 55°C/W			128°C/W 55°C/W			



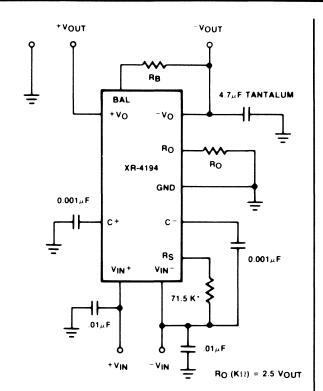




For Best Tracking Temperature Coefficient of R<sub>O</sub> Should Be Same As For R<sub>S</sub>

Adjust R<sub>O</sub> for V<sub>S</sub> 6 V (15 KΩ) then Adjust R<sub>B</sub> for V<sub>S</sub> 12 V (20 KΩ)

Figure 1. Typical Applications





# ±15V Dual-Tracking Voltage Regulator

# **GENERAL DESCRIPTION**

The XR-4195 is a dual-polarity tracking regulator designed to provide balanced positive and negative 15V output voltages at currents of up to 100 mA.

The device is ideal for local "on-card" regulation, which eliminates the distribution problems associated with single-point regulation. Intended for ease of application, the XR-4195 requires only two external components for operation.

# **FEATURES**

Direct Replacement for RM/RC-4195 ± 15V Operational Amplifier Power Thermal Shutdown at T<sub>J</sub> = 175°C Output Currents to 100 mA Available in 8-Pin Plastic Mini-DIP Low External Pars Count

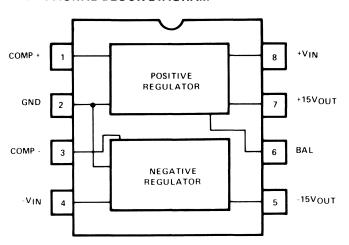
# **APPLICATIONS**

Operational Amplifier Supply On-Card Regulation Regulating High Voltage

# **ABSOLUTE MAXIMUM RATINGS**

Input Voltage  $\pm V$  to Ground  $\pm 30V$  Power Dissipation at TA = 25°C 600 mW Load Current 100 mA Operating Temperature Range 0°C to +125°C Storage Temperature Range -65°C to +150°C

# **FUNCTIONAL BLOCK DIAGRAM**



# ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-4195CP	Plastic	0°C to +70°C

# SYSTEM DESCRIPTION

The XR-4195 is a dual polarity tracking voltage regulator, internally trimmed to ±15V. Only output capacitors are required for operation. Internal protection circuits include thermal shutdown and active current limiting. The device may be configured as a signal output high voltage regulator by adding a voltage divider between an output pin, the device ground (Pin 2) and system ground.



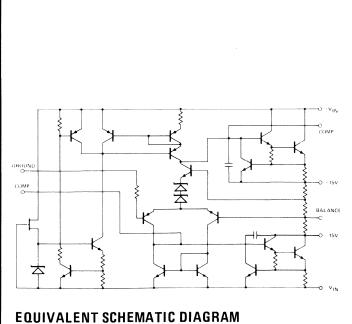
# **ELECTRICAL CHARACTERISTICS**

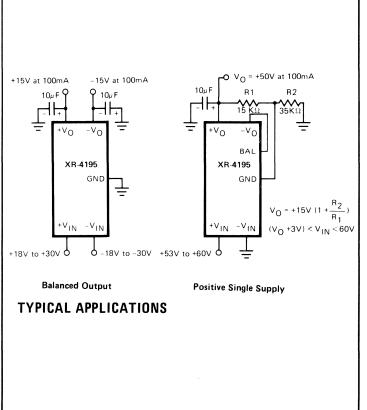
**Test Conditions:**  $I_L = 1 \text{ mA}$ ,  $V_{CC} = \pm 20 \text{V}$ ,  $C_L = 10 \,\mu\text{F}$  unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNIT	CONDITIONS
Line Regulation Load Regulation Output Voltage Temperature Stability Standby Current Drain Input Voltage Range Output Voltage Output Voltage Tracking Ripple Rejection Input-Output Voltage Differential Short-Circuit Current Output Noise Voltage	18 14.5	2 5 0.005 ±1.5 15 ±50 75 220 60	20 30 0.015 ±3.0 30 15.5 ±300	mV mV %/°C m.4 V mA V mA	$V_{IN} = \pm 18 \text{ to } \pm 30V$ $I_{L} = 1 \text{ to } 100 \text{ mA}$ $V_{IN} = \pm 30V, I_{L} = 0\text{mA}$ $T_{i} = \pm 25^{\circ}\text{C}$ $f = 120 \text{ Hz}, T_{i} = \pm 25^{\circ}\text{C}$ $I_{L} = 50 \text{ mA}$ $T_{i} = \pm 25^{\circ}\text{C}$ $T_{i} = \pm 25^{\circ}\text{C}$
Internal Thermal Shutdown		175		°C	f = 100 Hz to 100 kHz

# THERMAL CHARACTERISTICS

	XR-4195CP			
PARAMETERS	MIN.	TYP.	MAX.	CONDITIONS
Power Dissipation			0.6W	T <sub>A</sub> = 25° C T <sub>C</sub> = 25° C
Thermal Resistance		210°C/W		Τ <sub>C</sub> = 25°C <i>θ</i> J-C
Thornial Hospitalios		2.0 0,		<b>θ</b> J-A







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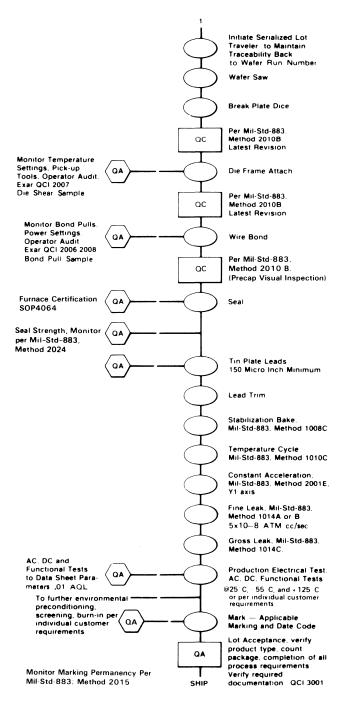
# **EXAR** Quality Assurance Standards

The quality assurance program at EXAR Corporation defines and establishes standards and controls on manufacturing, and audits product quality at critical points during manufacturing. The accompanying Manufacturing/QA process flow charts illustrate where quality assurance audits the manufacturing process, by inspection or test. The insertion of these quality assurance points is designed to insure that the highest quality standards are maintained on EXAR products during manufacturing. Realizing that these standard Manufacturing/QA process flows do not meet the needs of every customer requirement, EXAR Quality Assurance will negotiate any additional screening needs to meet any individual customer's specific requirement.

#### Wafer Fabrication/QA Flow

# Polished Silicon Slices er Applicable Per Applicable QC QC. QA MQCI's MQCI's Specification, MQCI's Oxidation Diffusion QA. QC Visual Inspection for Contamination, etc. **Epitaxial Layer** Verify Laver Thickness and Resistivity QΑ Inspect for Stacking Faults, etc. Diffusion oc Masking Visual Inspection to Verify Proper Mask QΑ Check Alignment, Undercutting, Proper QC Oxide Removal, etc. Aluminum Evaporation QC QA S.E.M. Analysis Individual Wafer S.E.M. Analysis (optional for high reliability military programs only Glassivation QΑ QC Wafer probe 100% probe AC, DC, and Functional Testing Die Sort Yield Analysis (optional, for high reliability military programs only) Move to Assembly High Reliability Cerdip Plastic Assembly Assembly

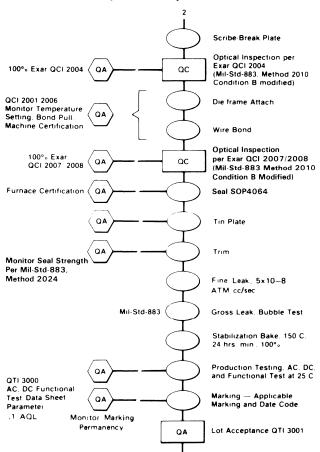
# High Reliability Assembly/QA Flow



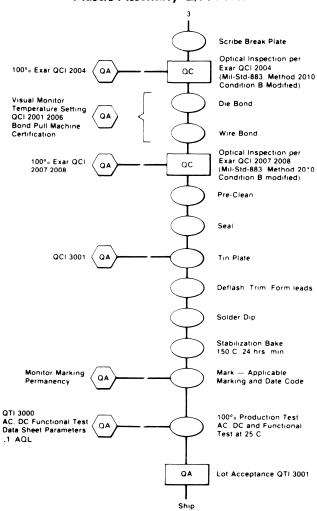
3



# Cerdip Assembly Q/A Flow



# Plastic Assembly Q/A Flow



# PRODUCT ORDERING INFORMATION

Ship

**XXXXX** 

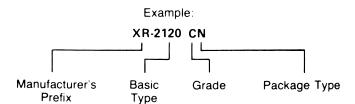
Basic Type

#### Part Identification

#### XR Manufacturer's Prefix Grade Package Type M = Hi-Rel N = Ceramic Dual-in-line Prime = Plastic Dual-in-line Ν Electrical MD = Small Outline Prime Electrical

Commercial

---Kit



# **Definition of Symbols:**

= Hi-Rel Grade Part, Ceramic Package Only, and are guaranteed to operate over the temperature range of  $-55^{\circ}$  to  $+125^{\circ}$ C.

= Prime Grade Part, Ceramic Package. N = Prime Grade Part, Plastic Package.

CN = Commercial Grade Part, Ceramic Package.

CP = Commercial Grade Part, Plastic Package.

= Commercial Grade Part, Plastic Small Outline Package MD (Marking does not include MD letters)

N, P, CN and CP parts are electrically identical and guaranteed to operate over 0°C to + 70°C range unless otherwise stated. In addition, N and P parts generally have operating parameters more tightly controlled than the CN or CP parts.

For details, consult Exar Sales Headquarters or Sales /Technical Representatives.

### Legend:

	Operation	100% inspection
74	Surveillance	QC = Quality Control QA = Quality Assurance



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This single volume data book combines all of EXAR's catalogs (see below) into one easy-to-use, comprehensive publication. The book contains a complete summary of technical information covering EXAR's full line of standard, custom and semi-custom IC products.

#### STANDARD PRODUCT GUIDE

A complete short-form catalog of all of EXAR's standard products, quality assurance programs and technical capabilities. Key features and applications of each of EXAR's products are given, along with their functional block diagrams, package types, and operating temperature ranges. Products are grouped according to their applications, and a complete industry-wide cross reference chart is provided.

#### **CUSTOM AND SEMI-CUSTOM PRODUCT GUIDE**

This book contains a complete outline and summary of EXAR's unique custom and semi-custom IC design, development, and production capabilities. Full custom and semi-custom programs which offer unique and effective methods of manufacturing an almost unlimited variety of custom linear or digital monolithic ICs is included as well as packaging information and Quality Assurance Program information.

#### MODEM DESIGN HANDBOOK

This publication includes all EXAR data sheets and application notes relating to Modem products as well as a section on Modem fundamentals. Subjects covered in this fundamentals section include: Modulation and Demodulation techniques for both FSK and PSK systems, filter considerations, line interface, and test modes. The scope of this manual allows even the beginning modem designer to implement EXAR's available integrated circuits into complete working modems.

# SWITCHING REGULATOR DATA BOOK

EXAR's entire line of switching regulator IC products are specified in this technical data book. In addition, several design and application articles are included, along with a review of the fundamentals of pulse-wide modulated regulator circuits.

#### PHASE-LOCKED LOOP DATA BOOK

The fundamentals of design and application of monolithic phaselocked loop (PLL) circuits are included in this data book. A long list of PLL applications are illustrated covering FM demodulation, frequency synthesis, FSK, and tone detection. Particular emphasis is given to the application of PLL circuits in data interface and communication systems such as FSK Modems. This book also contains the data sheets and electrical specifications for all of EXAR's PLL products.

#### **OPERATIONAL AMPLIFIER DATA BOOK**

A collection of technical articles on the fundamentals of monolithic IC op amps is contained in this technical publication. Some of the basic op amp circuits are given, and the application of IC op amps in active filter design is discussed. A complete set of electrical specifications on EXAR's bipolar and BIFET op amp products is included.

#### TIMER DATA BOOK

Provided in this publication is a collection of technical articles and application information on monolithic timer IC products. Also included are the data sheets and detailed electrical specifications for all of EXAR's timer circuits, including the programmable timer/ counter, micropower, and long-delay timers.

#### **FUNCTION GENERATOR DATA BOOK**

This comprehensive data book contains a number of technical articles and application notes on monolithic voltage-controlled oscillators (VCO), and function generator IC products. In addition, the data sheets and technical specifications for EXAR's monolithic VCO's and function generators are included.

#### **APPLICATIONS DATA BOOK**

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